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A Radiation Hardened by Design Technique for DPLL Using 45nm-SOI Technology

Sapate Shraddha, Verma Arpana and Sahu Thaneshwar

UTD, CSVTU, Bhilai, Chhattisgarh, India.
Email; Shraddhasapate7@gmail.com, arpanaverma91@gmail.com
Ph.+91-8962475225, +91-7987785556

ABSTARCT

Radiation hardening is the process of making electronic devices and systems resistant of damage or malfunctions due to the striking or hitting of charge particles or ions. These charge particles identified at space area and nuclear areas due to the presence of x-rays, gamma rays, protons, neutrons, alpha particles etc. Due to the hitting of charge particles on the electronic components either soft or hard error generated this error can create temporary or permanent damage to the device. A single charge particle itself can destroy the whole lattice structure of an electronic device due to losing numbers of electrons at a time. PLL is second order system which is used for generation of multiple frequencies at a time and mainly used in space areas in satellites. Due to the critical charge insertion the performance of PLL may degrade. The critical charge in PLL can create either SEU (single event upset) or SET (single event transients). Where SEU is used to indicate the soft error (flipping or losing of data) and SET is used to indicate the error causes in analog circuitry. To avoid this issue a radiation hardened by design PLL is approached by using 45nm silicon-on-insulator (SOI) technique. All performances are simulated, tested and verified using HSPICE tool presented by Synopsys.

KEYWORDS: SET (single event transient), critical charge, PLL, RHBD (radiation hardened by design), SEU (single event upset).

***Corresponding author**

Shraddha Sapate

UTD, CSVTU, Bhilai, Chhattisgarh, India.

Shraddhasapate7@gmail.com +91-8962475225

INTRODUCTION

PLL is a system generally used for generation of multiple frequencies and synthesizing of frequencies. Widely it is used in space areas for satellites, nuclear reactors, military purpose in radio and telecommunication fields. With perpetual scaling of device, lowering of the power supply for achievement of higher frequencies, VLSI circuits become more unreliable and unprotected and create cross talk due to noise present in supply voltage[1, 2]. It creates issues such as SEEs (single event effects) or soft errors.

In a VLSI design system SEE or soft errors caused due to the radiation of charge particles such as alpha, gamma, neutrons, protons etc. this causes the glitches (voltage glitch) on the affected node due to the deep penetration of charge particles presented in the device. Due to this flipping of data (0 to 1 or 1 to 0) occurs in a memory elements and result a single event upset (SEU), where SEU persuade errors in sequential elements continue to be problematic[3]. The combination of errors due to the particle strike can result an improper wrong data latched with sequential elements and can create either single or multiple node upsets. Such radiation striking happens in combinational circuits known as single event transient (SETs). Previously various works has been proposed for implementation of radiation hardened by design PLL[4]. TMR based PLL has been approached in which they triplicate the oscillator circuitry to achieve high redundancy and radiation tolerance. But this requires large area which consumes more power [5]. The voltage based charge pump instead of current based charge pump but this methodology is not sufficient to protect over all PLL circuitry[6]. The separation of gate input for both nmos and pmos so that 0 to 1 flipping or 1 to 0 flipping will not affect the overall performance of PLL but the circuitry of oscillator in this PLL causes large delay[7].

RHBD PLL

PLL is a second order system generally used for generation of multiple frequencies. For implementation of radiation hardened by design PLL differentiating the gate inputs to protect the device from SEU for nmos and pmos. By this methodology we can achieve a radiation tolerance PLL up to 100pC. The block diagram of general digital PLL is shown in Fig. 1. The PLL consists of a sequential phase frequency detector implemented by using D Flip-Flops for detection of the difference between data reference and feedback clock, a voltage based charge pump for conversion of digital output voltage of phase frequency detector to analog voltage, a loop filter for filtering the unwanted glitches from the output of charge pump, a voltage controlled oscillator for generation of clock frequency and a frequency divider circuit for dividing the clock according to requirement[8, 9].

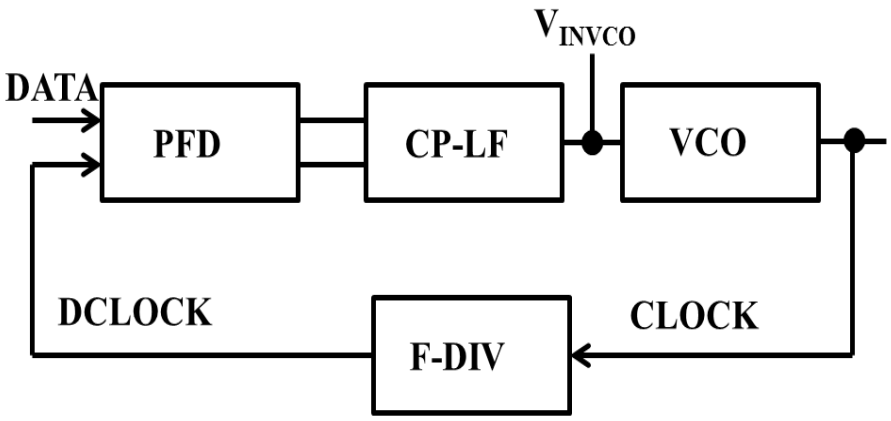
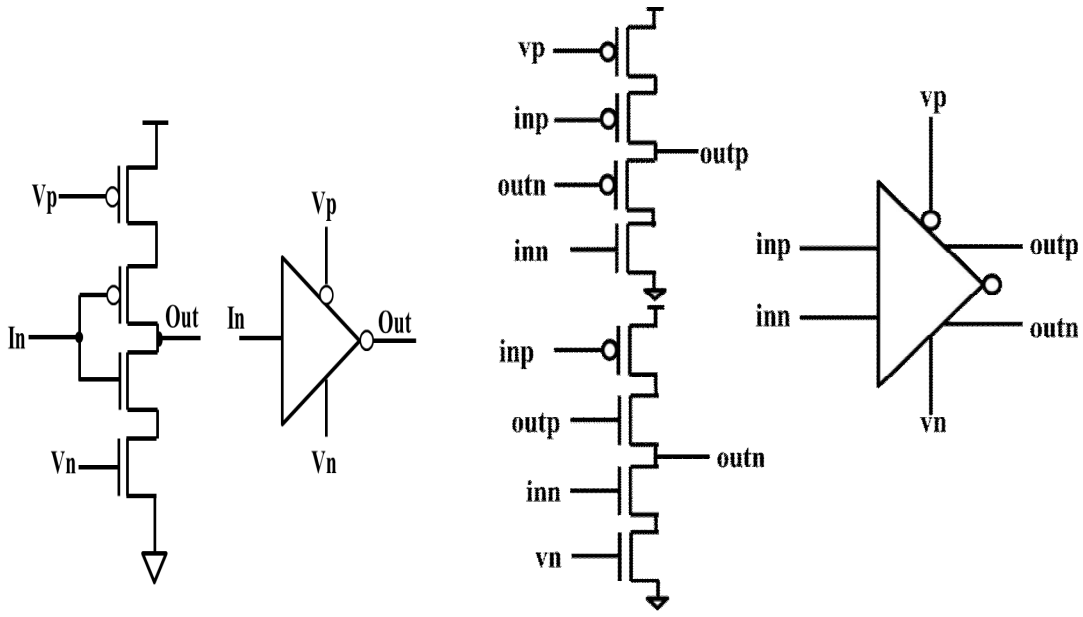


Fig. 1 Block diagram representation of DPLL

As by the study it is observed that the most SEE (single event effect) sensitive area is the input and output of VCO (voltage controlled oscillator) and LF (loop filter) respectively. To reduce the sensitivity of this node the separation of gate input for implementation of radiation hardened by design VCO has been performed[10,11].

METHODOLOGY FOR RHBD VCO

We implemented a voltage controlled oscillator which requires a current starving inverter. The current starving inverter is used to reduce the drain current leakage of the inverter circuit. The basic current starving inverter required two nmos and two pmos joined with each other shown in Fig.2 (a). To improve the circuit for making as radiation tolerance some modification has been done on the basic current starved circuit shown in Fig.2 (b).



(a) **(b)**

Fig. 2 (a) Unhardened current starved inverter, (b) Hardened current starved inverter

Fig. 2 (b) represents the modified circuitry of current starved ring inverter as compare to Fig. 2 (a) the symbolic representation of hardened and unhardened also mentioned in Fig. 2 (a) and 2 (b) respectively. By separating the input we reduced the possibilities of data flipping (which is from 0 to 1 for nmos and 1 to 0 for pmos).

RESULT AND ANALYSIS OF PLL

For analysis of radiation hardened by designed PLL here we are using HSPICE tool using PTM model card of 45nm-SOI (FinFET) technology. In the modern era to achieve high gain with low power consumption device downscaling is a common process. Where instead of traditional cmos silicon-on-insulator (SOI) based MOSs is implemented to achieve high performance. SOI can be used in both either low frequencies or in high frequencies. It has high noise rejection ratio and provide low power dissipation as compare to traditional cmos. While using 45nm technology we achieved the center frequency up to 0.765GHz. For calculation of frequency the given eq. 1 as shown below[12]:

$$f_{osc} = \frac{I_D}{N.VDD.C_{tot}} \quad 1$$

Where, f_{osc} = center frequency of PLL.

N = number of VCO inverter stage.

VDD = DC power supply.

C_{tot} = total capacitance of PLL.

The number of VCO inverter stage can be decide according to the requirement of frequency[13], the supply voltage VDD here is 0.9V and the total capacitance value for SOI based cmos is 0.554 fF. During simulation I_d current measured as 8 μA.

A. Transfer Characteristics for VCO frequency: For analysis of frequency transfer characteristics, we did Monte Carlo simulation by taking 1000 samples using 3σ process variation as Gaussian distribution. The graph required for frequency response of both unhardened and hardened PLL shown in Fig. 3.

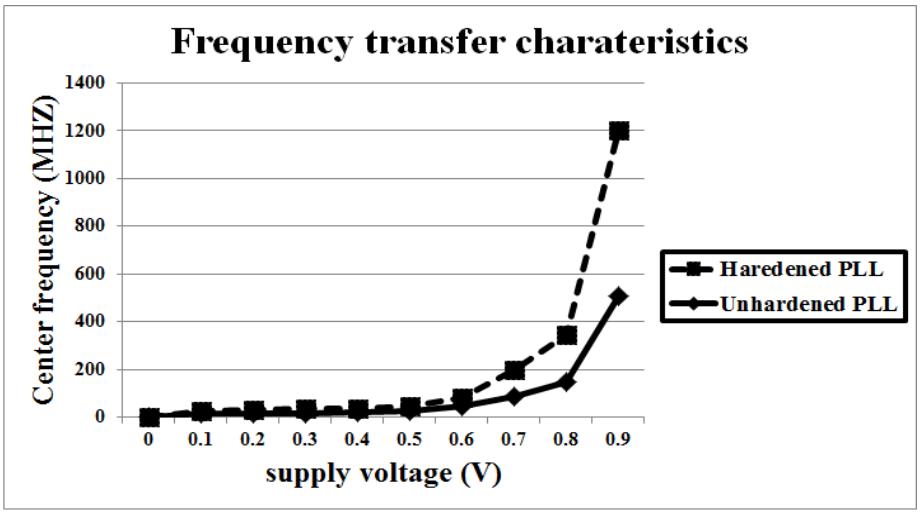


Fig. 3 frequency transfer characteristics response of unhardened and hardened PLL.

The graph presented in Fig. 3 shows the center frequency of both hardened and unhardened at different threshold voltage levels of MOS. Where up to the range of 0.4V to 0.6V the DPLL is in lock range where the high range of frequency can be achieved. It is known that the performance of ring based oscillator is high as compare to the LC tank based oscillators. Due the high tuning range with high noise immunity and low area consumption ring based oscillator is used. Ring based oscillator is easy to fabricate and it requires less area as compared LC-tank based oscillators.

B. VCO response for PLL: The output response of PLL is shown in Fig. 4. The VCO response is categorized into two range lock range and capture range.

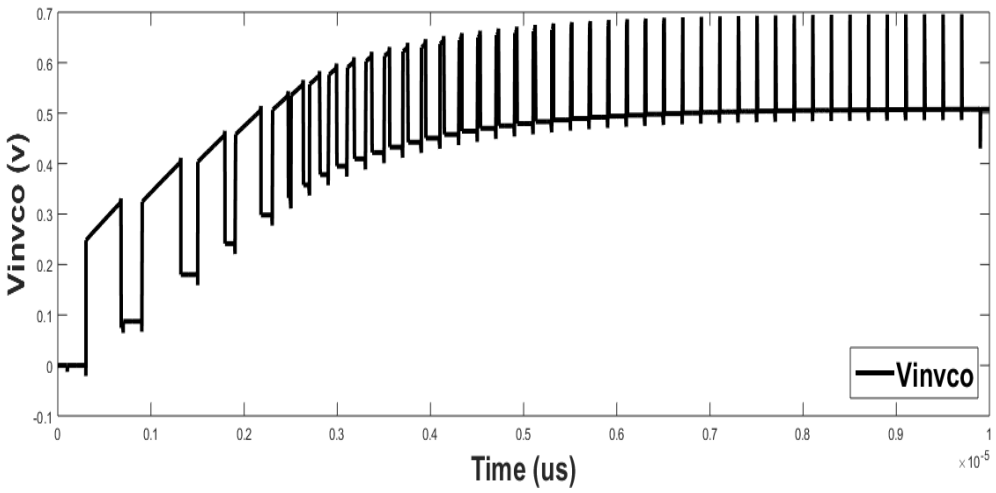


Fig. 4 Output response of VCO

Capture range is defined for the range at which the PLL starts responding to match the frequencies. Lock range defines the matched frequencies of PLL.

C. Delay analysis: The delay analysis of the different PLL has been done and presented in Table 1 Where the two different radiation-hardened PLL has been compared with unhardened PLL.

Table No. 1 "Delay analysis of various PLLs"

Types of PLL	Technology (nm)	Delay (µs)
Unhardened PLL	45-nm cmos	1.6545
TMR-PLL	45-nm SOI	1.562
RHBD-PLL	45-nm SOI	1.17

The Table 1 represents the delay of three types of PLL where due to redundancy in design the delay of proposed (RHBD-PLL) methodology has been reduced.

CONCLUSION

The proposed technique for implementation of Radiation Hardened PLL for minimization of SET is experimentally verified. The Monte Carlo simulation for frequency transfer characteristics has been performed which indicates the increased tuning range of frequency for RHBD-PLL with less delay at the cost of using more number of transistors. Due to the replacement of traditional CMOS with FinFET the power and delay of the proposed RHBD-PLL has been reduced. As FinFET provides less leakage of current as compare to CMOS it provides high performance for high

frequency based circuits e.g. PLL. By modifying the VCO circuit the mitigation of SET is possible for multimode upset as compare to single node upset in future work.

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