

## *International Journal of Scientific Research and Reviews*

### **Single Input DC to Multiple Output DC Buck Converter**

**K. Ravi Kumar<sup>1</sup> and M. Sai Kumar<sup>2\*</sup>**

<sup>1</sup>Associate Professor, Electrical and Electronics Engineering, Vasavi College of Engineering, Hyderabad, Telangana, India.

<sup>2</sup>PG Scholar, Electrical and Electronics Engineering Vasavi College of Engineering, Hyderabad, Telangana, India,  
[ravikadali12345@rediffmail.com](mailto:ravikadali12345@rediffmail.com)<sup>1</sup>, [muthyalasaiyadav033@gmail.com](mailto:muthyalasaiyadav033@gmail.com)<sup>2</sup>

---

#### **ABSTRACT**

This paper proposes a new single-input three-output DC-DC buck converter. The proposed topology has single input DC to multiple output dc-dc converter which has two less switching devices than that of a conventional converter. This decrease in switching devices leads to lesser cost and a more even division of power losses among the switching devices. A comprehensive small signal Modeling and control strategies for the dc-dc converter will be presented. Simulation and experimental results are presented to validate the theoretical expectations. The simulation is performed using PSIM.

**KEYWORDS:** AC-DC converter, DC-DC buck converter, bidirectional, unidirectional, small signal analysis.

---

**\*Corresponding Author:**

**M. Sai Kumar**

PG Scholar, Electrical and Electronics Engineering Vasavi College of Engineering,  
Hyderabad, Telangana, India,

E Mail - [muthyalasaiyadav033@gmail.com](mailto:muthyalasaiyadav033@gmail.com)

## INTRODUCTION

Applications of DC-DC converters include renewable energy systems<sup>1</sup>, hybrid electric vehicles<sup>5, 6</sup>, and uninterrupted power supplies<sup>7,8</sup>. DC-DC converters can be made with both unidirectional and bidirectional power flow capabilities<sup>1-4</sup>. The unidirectional converter is made using a power switch, a power diode, and an *LC* filter<sup>1-3, 14</sup>. The bidirectional converter is achieved by removing the power diode and placing a power switch in parallel with the *LC* filter. Fig. 1(a) shows that by replicating the bidirectional circuit three times, a bidirectional single-input three-output converter can be achieved. In<sup>13</sup>, bidirectional DC-DC converters were shown to require smaller sized filters than that of a unidirectional converter. Faster dynamic response and lower device stress were also noted in the bidirectional converter<sup>13</sup>. In<sup>12</sup>, a bidirectional DC-DC converter topology was proposed for use in applications that do not require magnetic components.

Applications such as communication systems and battery management systems require a DC-DC buck converter with multiple controlled outputs. In<sup>17</sup>, a configuration was proposed that uses a single inductor for obtaining three controlled outputs. A three switch DC-DC buck converter topology was proposed in<sup>18</sup> that can be used in applications that require two controlled outputs. In this paper, a novel single-input three-output DC-DC buck converter has proposed. The proposed topology requires two fewer power switches than that of the conventional single-input three-output DC-DC buck converter. The differences of these converters are highlighted in Fig. 1.

## PROPOSED CONVERTER

The proposed topology consists of four power switches (*S1*, *S2*, *S3*, and *S4*) and three low pass filters (*L1-C1*, *L2- C2*, and *L3-C3*). The state of the each switch is represented by binary variables, that is,  $q_x= 0$  indicates that switch *S<sub>x</sub>* is OFF, and  $q_x= 1$  indicate switch *S<sub>x</sub>* is ON, where  $x=1, 2, 3$ , and 4. Since there are four switches and two states for each switch, we attain 16 ways of operating the converter. Of these 16 states, only four are operational. All the other switching combinations should be avoided because in that particular instant output of any one of the load is discontinuous. Table 1 provides the topological states (TS) where TS-1, TS-2, TS-3, and TS-4 represent the operational states. It can be observed from Fig.2 that:

For TS-1 ( $q_1 = 0, q_2 = 1, q_3 = 1, \text{ and } q_4 = 1$ ), the input energy is supplied to all the loads and inductors. This means inductors *L1*, *L2*, and *L3* will be charged (see Fig. 2(b)).

For TS-2 ( $q_1 = 1, q_2 = 0, q_3 = 1,$  and  $q_4 = 1$ ), the input energy is provided to  $R_1, L_1,$   $R_2,$  and  $L_2$ . Energy stored in inductor  $L_3$  is dissipated. In Fig. 2(b),  $i_{L3}$  flows in the closed path formed by switch  $S_4$ .

For TS-3 ( $q_1 = 1, q_2 = 1, q_3 = 0,$  and  $q_4 = 1$ ), the input energy is provided to  $R_1$  and  $L_1$ . Energy stored in inductors  $L_2$  and  $L_3$  is dissipated. This means the current  $i_{L2}$  will be flowing in the closed path (see Fig. 2(c)) formed by switch  $S_3$  and  $S_4$ , and current  $i_{L3}$  will be flowing in the closed path formed by switch  $S_4$ .

Finally, in TS-4 ( $q_1 = 1, q_2 = 1, q_3 = 1,$  and  $q_4 = 0$ ), energy provided to all the inductors dissipates to their respective loads. Currents  $i_{L1}, i_{L2},$  and  $i_{L3}$  are discharged during this state (see Fig. 2(d)).

Table-1 Topological states

q1	1	1	1	0
q2	1	1	0	1
q3	1	0	1	1
q4	0	1	1	1
Topological states	TS-1	TS-2	TS-3	TS-4

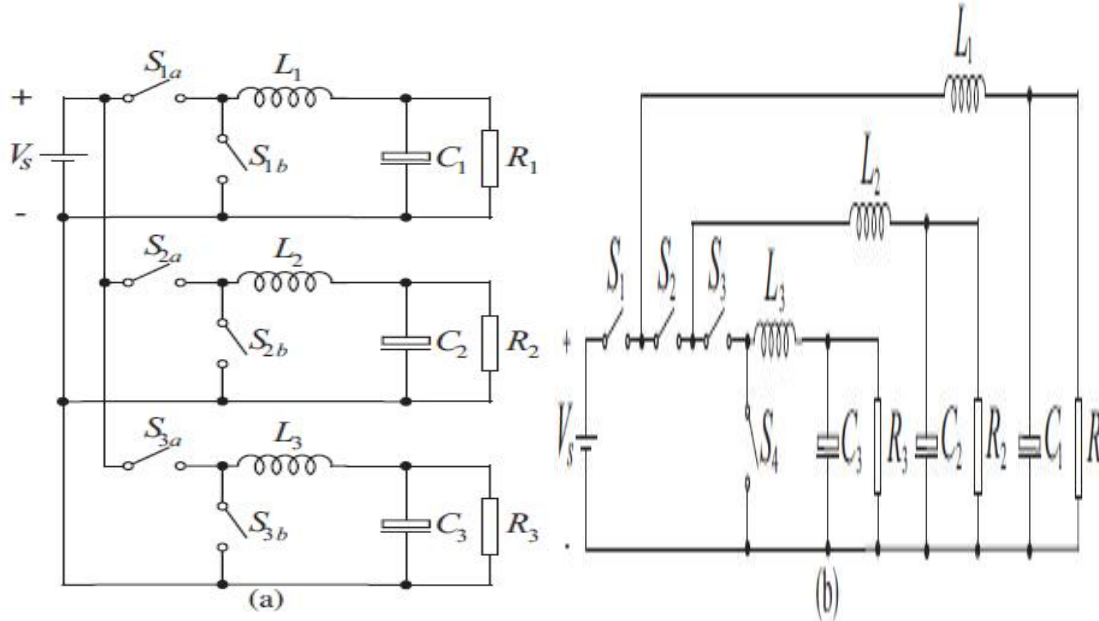


Fig. 1. Synchronous single-input multiple-output DC-DC converter for (a) conventional topology, and (b) the proposed topology.

## STEADY STATE ANALYSIS

The proposed converter is assumed to be operating in continuous conduction mode with inductor waveforms shown in Fig. 3(a). From the waveforms and topological states obtained in the preceding sections, it can be deduced that variable  $V_{R1}$  controls output voltage  $V_{o1}$ , variable  $V_{R2}$  controls output voltage  $V_{o2}$ , and variable  $V_{R3}$  controls output voltage  $V_{o3}$ . Since the average inductor voltage is zero, the following equations can be obtained:

$$(V_s - V_{o1})T_{on1} = V_{o1} (T_s - T_{on1}) \quad (1)$$

$$(V_s - V_{o2}) (T_s - T_{on2}) = V_{o2}T_{on2} \quad (2)$$

$$(V_s - V_{o3}) (T_s - T_{on3}) = V_{o3}T_{on3} \quad (3)$$

Here  $T_{on1}$ ,  $T_{on2}$ , and  $T_{on3}$  are the time periods for the duration of which respective PWM generators 1, 2, and 3 are producing logic “1” at their output.

From the above equations, the output voltages can be derived as a function of their duty cycles and supply voltage. The output voltages are represented by the following equations

$$V_{o1} = (D_{gen1})V_s. \quad (4)$$

$$V_{o2} = (1 - D_{gen2})V_s. \quad (5)$$

$$V_{o3} = (1 - D_{gen3})V_s. \quad (6)$$

where  $D_{gen1}$ ,  $D_{gen2}$ , and  $D_{gen3}$  represent the duty cycles.

## INDEPENDENT OUTPUT VOLTAGE GENERATION

The duty cycle of switch  $S_1$  can be ranging from a minimum value of 0 to a maximum value of 1. Assuming the duty cycle for switch  $S_1$  is  $D_1 = 3/4$ , the output voltage on load 1 would be 75% of the input voltage. The duty cycle of switch  $S_2$  can be ranging from 0 to  $D_1$ . Similarly, the duty cycle of the switch  $S_3$  can be ranging from 0 to  $D_2$ . As a consequence, the output voltage across load 1 is always higher than the voltage across load 2, and the output voltage across load 2 is always higher than the output voltage across load 3. In conventional converters, the output voltage at each load can be varied by varying their respective duty cycles from 0 to 1. This means  $0 < D_1 < 1$ ,  $0 < D_2 < 1$ , and  $0 < D_3 < 1$ .

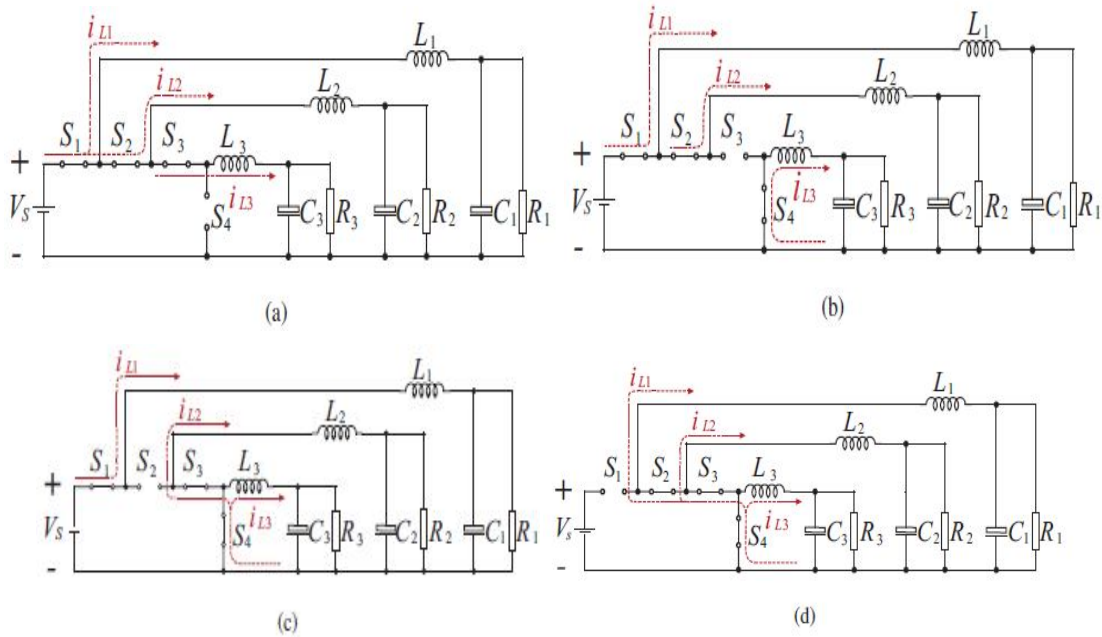


Fig. 2. Modes of operation: (a) TS-1, (b) TS-2, (c) TS-3, and (d) TS-4.

## PULSE WIDTH MODULATION

The four switches discussed in the preceding section are operated using pulse width modulation (PWM) technique. This modulation approach deals with a comparison of reference voltages  $V_{R1}^*$ ,  $V_{R2}^*$ , and  $V_{R3}^*$  with a saw-tooth waveform. The output of this comparison goes through a logic circuit which dictates the state of the switches. These reference voltages will control the output voltages across  $R_1$ ,  $R_2$ , and  $R_3$ . Note that the output of the first PWM generator will be the difference between the saw-tooth waveform and  $V_{R1}^*$ . Likewise, the output of the second and third PWM generator will be obtained with respect to  $V_{R2}^*$ , and  $V_{R3}^*$  respectively.

The PWM logic circuit realization is shown in Fig. 3(d) is used for controlling the duty cycle of the switches. This circuit is built, based on few conclusions that were developed from the operation of the converter described during its corresponding topological state.

The charging of inductor  $L_1$  is entirely dependent on switch  $S_1$ . Hence, the first PWM generator can be directly connected to switch  $S_1$  to control the output voltages  $V_{O1}$  or the state of inductor  $L_1$ .

During the topological state (TS-4), switch  $S_2$  is “ON,” at the same time, inductor  $L_2$  is discharging during this period. This means that the charging and discharging of the

inductor  $L_2$  is not dependent on the state of the switch  $S_2$ . Note that, switch  $S_2$  should be operated in such a way that topological states TS-1 and TS-2 remain for an interval that can be defined by the second PWM generator. In addition, switch  $S_2$  should be controlled in such a way that prohibited states are avoided. These requirements are achieved by using a two input “OR” gate and a “NOT” gate shown in Fig. 3(c).

By similar observation, switch  $S_3$  should be operated in such a way that topological state TS-1 remains for an interval of time that is defined by third PWM generator. Switch  $S_3$  should also be controlled in such a way that, it stays “ON” when either of switches  $S_1$  or  $S_2$  turns “OFF.” These requirements can be satisfied by using a three input “OR” gate in which, the output of third PWM generator and the inverse of the first and second generators are connected.

Finally, switch  $S_4$  defined by the state of the switches  $S_1$ ,  $S_2$ , and  $S_3$ . This means that the function of switch  $S_4$  in the circuitry is to avoid the prohibited states. This control of the switch can be achieved by using a “NAND” gate. Fig. 3(c) shows the gating signals that are obtained for switches  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$  respectively.

## SMALL SIGNAL ANALYSIS

In the case of designing a controller or assessing the performance for a converter, the linearization techniques discussed in<sup>19</sup> can be used. In order to have a clear understanding on the dynamics of the novel configuration, small signal analysis is performed and transfer functions are derived. Following the procedure outlined in<sup>20</sup>. Kirchoff’s laws is applied on the topological states, and their corresponding equations are as follows:

### Topological state-1:

$$L_1 \frac{di_{L1}}{dt} + V_{01} = V_s \quad (7)$$

$$L_2 \frac{di_{L2}}{dt} + V_{02} = V_s \quad (8)$$

$$L_3 \frac{di_{L3}}{dt} + V_{03} = V_s \quad (9)$$

$$C_1 \frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \quad (10)$$

$$C_2 \frac{dV_{02}}{dt} + \frac{V_{02}}{R_2} = i_{L2} \quad (11)$$

$$C_3 \frac{dV_{03}}{dt} + \frac{V_{03}}{R_3} = i_{L3} \quad (12)$$

**Topological state-2:**

$$L_1 \frac{di_{L1}}{dt} + V_{01} = V_s \quad (13)$$

$$L_2 \frac{di_{L2}}{dt} + V_{02} = V_s \quad (14)$$

$$L_3 \frac{di_{L3}}{dt} + V_{03} = 0 \quad (15)$$

$$C_1 \frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \quad (16)$$

$$C_2 \frac{dV_{02}}{dt} + \frac{V_{02}}{R_2} = i_{L2} \quad (17)$$

$$\frac{V_{03}}{R_3} - C_3 \frac{dV_{03}}{dt} = i_{L3} \quad (18)$$

**Topological state-3:**

$$L_1 \frac{di_{L1}}{dt} + V_{01} = V_s \quad (19)$$

$$L_2 \frac{di_{L2}}{dt} + V_{02} = 0 \quad (20)$$

$$L_3 \frac{di_{L3}}{dt} + V_{03} = 0 \quad (21)$$

$$C_1 \frac{dV_{01}}{dt} + \frac{V_{01}}{R_1} = i_{L1} \quad (22)$$

$$\frac{V_{02}}{R_2} - C_2 \frac{dV_{02}}{dt} = i_{L2} \quad (23)$$

$$\frac{V_{03}}{R_3} - C_3 \frac{dV_{03}}{dt} = i_{L3} \quad (24)$$

**Topological state-4:**

$$L_1 \frac{di_{L1}}{dt} + V_{01} = 0 \quad (25)$$

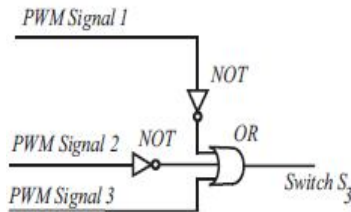
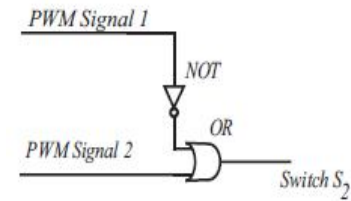
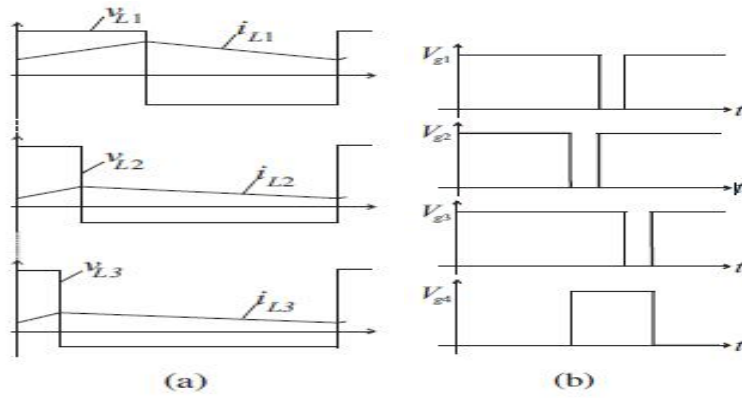
$$L_2 \frac{di_{L2}}{dt} + V_{02} = 0 \quad (26)$$

$$L_3 \frac{di_{L3}}{dt} + V_{03} = 0 \quad (27)$$

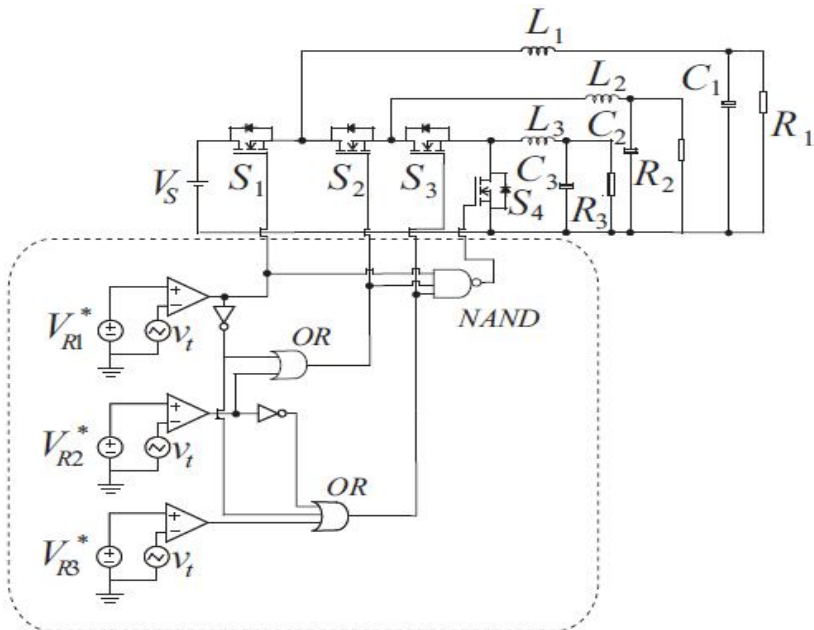
$$\frac{V_{01}}{R_1} - C_1 \frac{dV_{01}}{dt} = i_{L1} \quad (28)$$

$$\frac{V_{02}}{R_2} - C_2 \frac{dV_{02}}{dt} = i_{L2} \quad (29)$$

$$\frac{V_{03}}{R_3} - C_3 \frac{dV_{03}}{dt} = i_{L3} \quad (30)$$



(c)



(d)



Fig. 3. (a) Voltage and current waveforms for  $L_1$ ,  $L_2$ , and  $L_3$ , (b) Gating signal for switches  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$  respectively, (c) Logic circuits for defining the state of switches  $S_2$ , and  $S_3$ , (d) PWM implementation for the proposed topology.

The above equations are expressed in the form of state space equations and their resultant state space matrices are represented below. Here,  $A_1$ ,  $B_1$ , and  $C_1$  are the state space matrices which are obtained for the topological state-1. Similarly, the corresponding state space equations for TS-2, TS-3, and TS-4 were also derived and are as follows:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & 0 & 0 & \frac{-1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{-1}{R_2 C_2} & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & \frac{-1}{R_3 C_3} \end{bmatrix} \quad (31)$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & 0 & 0 & \frac{-1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{1}{C_2} & 0 & 0 & \frac{1}{R_2 C_2} & 0 \\ 0 & \frac{-1}{C_3} & 0 & 0 & 0 & \frac{1}{R_3 C_3} \end{bmatrix} \quad (32)$$

$$A_3 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{1}{C_1} & 0 & 0 & \frac{1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{-1}{C_2} & 0 & 0 & \frac{1}{R_2 C_2} & 0 \\ 0 & 0 & \frac{-1}{C_3} & 0 & 0 & \frac{1}{R_3 C_3} \end{bmatrix} \quad (33)$$

$$A_4 = \begin{bmatrix} 0 & 0 & 0 & \frac{-1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_2} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_3} \\ \frac{-1}{C_1} & 0 & 0 & \frac{1}{R_1 C_1} & 0 & 0 \\ 0 & \frac{-1}{C_2} & 0 & 0 & \frac{1}{R_2 C_2} & 0 \\ 0 & 0 & \frac{-1}{C_3} & 0 & 0 & \frac{1}{R_3 C_3} \end{bmatrix} \quad (34)$$

$$B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ \frac{1}{L_3} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad B_3 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad B_4 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (35)$$

$$C_1 = C_2 = C_3 = C_4 = [0 \quad 0 \quad 0 \quad 1 \quad 1 \quad 1] \quad (36)$$

From the topological states that were depicted in the Fig. 2, it is good to mention that the converter operates in these states for a definite period of time. If  $D_a, D_b, D_c,$  and  $D_d$  are considered as duty cycles for the respective topologies TS- 1, TS-2, TS-3, and TS-4. State space matrices for the whole converter are derived by adding the resultant matrices, which are obtained by multiplying the above state space matrices (31)-(34) with their corresponding topological duty cycles. Equations represented below are the state space equations for the proposed single input triple output DC-DC buck converter.

$$\frac{di_{L1}}{dt} = \frac{-(V_{01})}{L_1} + \frac{(T_1 + T_2 + T_3) V_s}{L_1} \quad (37)$$

$$\frac{di_{L2}}{dt} = \frac{-(V_{02})}{L_2} + \frac{(T_1 + T_2) V_s}{L_2} \quad (38)$$

$$\frac{di_{L3}}{dt} = \frac{-(V_{03})}{L_3} + \frac{(T_1) V_s}{L_3} \quad (39)$$

$$\frac{dV_{01}}{dt} = \frac{(T_1 + T_2 + T_3 - T_4) (i_{L1})}{C_1} + \frac{(T_1 + T_2 + T_3 - T_4) V_{01}}{R_1 C_1} \quad (40)$$

$$\frac{dV_{02}}{dt} = \frac{(T_1 + T_2 - T_3 - T_4) (i_{L2})}{C_1} + \frac{(T_1 + T_2 - T_3 - T_4) V_{02}}{R_2 C_2} \quad (41)$$

$$\frac{dV_{03}}{dt} = \frac{(T_1 - T_2 - T_3 - T_4) (i_{L3})}{C_1} + \frac{(T_1 - T_2 - T_3 - T_4) V_{02}}{R_3 C_3} \quad (42)$$

Laplace transformation is applied on the converter's state space equations, and transfer functions are derived. The obtained transfer functions are:

$$\frac{V_{01}(s)}{V_s(s)} = \frac{(D_a + D_b + D_c)(D_x) R_1}{S^2(R_1 L_1 C_1) + (L_1(D_x))S + (D_x)R_1} \quad (43)$$

$$\frac{V_{02}(s)}{V_s(s)} = \frac{(D_a + D_b)(D_y) R_2}{S^2(R_2 L_2 C_2) + (L_2(D_y))S + (D_y)R_2} \quad (44)$$

$$\frac{V_{03}(s)}{V_s(s)} = \frac{(D_a)(D_z) R_3}{S^2(R_3 L_3 C_3) + (L_3(D_z))S + (D_z)R_3} \quad (45)$$

Where  $D_x = (D_a + D_b + D_c - D_d)$ ,

$D_y = (D_a + D_b - D_c - D_d)$ , and

$D_z = (D_a - D_b - D_c - D_d)$

In order to express the output variables with respect to input and control parameters, topological duty cycles  $D_a$ ,  $D_b$ ,  $D_c$ , and  $D_d$  are correlated with the duty cycles generated by PWM generators 1, 2, and 3. Resultant expressions are programmed in the following equations.

$$D_a + D_b + D_c = D_{gen1} \quad (46)$$

$$D_a + D_b = D_{gen2} \quad (47)$$

$$D_a = D_{gen3} \quad (48)$$

Since the state space frequency of DC-DC converter is zero, by Substituting the above equations(46)-(48) in (43)-(45), the transfer functions can be minimized into the following expressions.

$$\frac{V_{01}(s)}{V_s(s)} = D_{gen1} \quad (49)$$

$$\frac{V_{02}(s)}{V_s(s)} = D_{gen2} \quad (50)$$

$$\frac{V_{03}(s)}{V_s(s)} = D_{gen3} \quad (51)$$

## COMPARISON OF SWITCHING LOSSES AMONG THE TOPOLOGIES

This section discusses the advantages and disadvantages of the proposed topology when it is compared with the traditional configuration. PSIM software offers thermal

modules that are used to calculate the losses. Specifically, the one used for this comparison was for the IRFP 460 MOSFET. Fig. 4(a) shows the total semiconductor losses for both topologies. It can be seen that under some load conditions, the proposed topology offers semiconductor losses that are better, poorer or even the same as for a conventional one. Even though it does not always offer better efficiency, the proposed circuit does offer better power loss distribution among the switches in every case, which can be seen by comparing Fig. 4(b) and 4(c). The proposed and conventional circuit were put under the exact same conditions during the tests, that is  $V_s = 300V$ ,  $L_1 = L_2 = L_3 = 0.001H$ , and  $C_1 = C_2 = C_3 = 0.00012F$ . Under load conditions of  $R_1 = R_2 = R_3 = 100\Omega$ , the conventional topology had 97% efficiency while the proposed converter had 96% efficiency. Under load conditions  $R_1 = 3000\Omega$ ,  $R_2 = 2000\Omega$ , and  $R_3 = 50\Omega$ , the conventional topology had an efficiency of 91%, and the proposed topology had an efficiency of 93%. Both topologies operated at 94% efficiency under load conditions  $R_1 = 3000\Omega$  and  $R_2 = R_3 = 2000\Omega$ .

## **THERMAL ANALYSIS**

The junction temperature of the switches in both the proposed and traditional topology was simulated using an equivalent thermal circuit model. Fig. 5 shows this equivalent circuit for one of the switches. The three thermal resistances that are represented (from left to right) are; Thermal resistance junction to case ( $R_{JC}$ ), the thermal resistance of the thermal interface material ( $RTIM$ ), and thermal resistance of the heat sink ( $RH$ ). For simplification purposes, an only steady-state analysis was performed.

Both topologies were simulated under the conditions  $V_s=300V$ ,  $L_1 = L_2 = L_3 = 0.001H$ ,  $C_1 = C_2 = C_3 = 0.00012F$ ,  $R_1 = 3000\Omega$ ,  $R_2 = 2000\Omega$ ,  $R_3 = 50\Omega$ , ambient temperature=  $70^\circ F$ , and the impedance values  $R_{JC}$ ,  $RTIM$  and  $RH$  were taken to be 0.26, 0.1 and 0.35 respectively. As a matter of fact, a rise in temperature or the heat generated around the switch is directly proportional to the total losses of that corresponding switch. The proposed converter should operate at lower temperatures. But interestingly, temperatures among both configurations are similar, and they had an even distribution of heat among the switches.

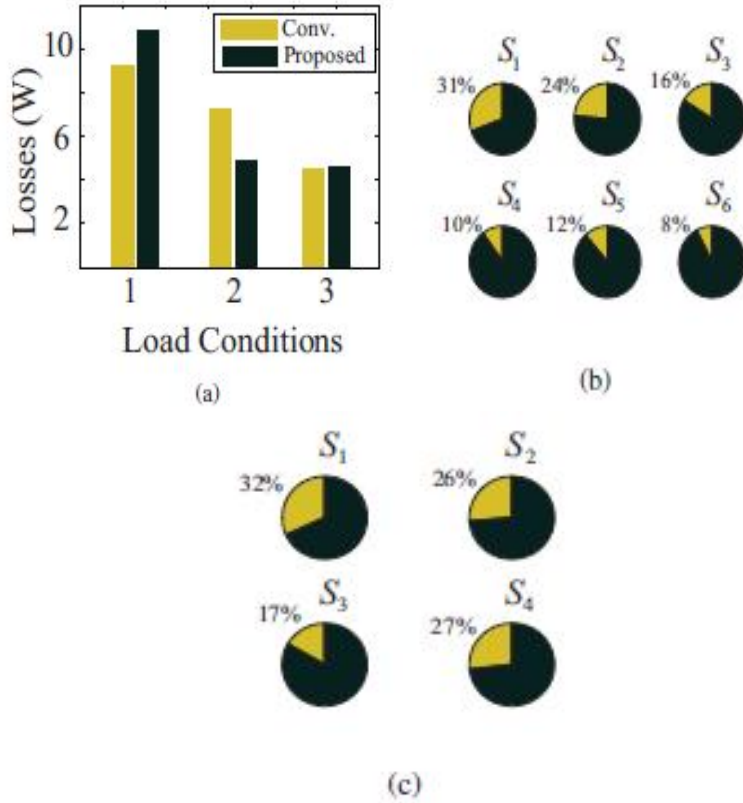


Fig. 4. (a) Semiconductor losses under different load conditions, (b) Traditional semiconductor loss distribution. (c) Proposed semiconductor loss distribution.

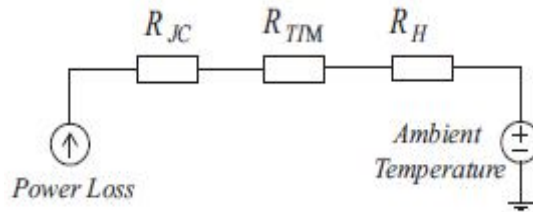


Fig. 5. Equivalent thermal model

Table 2 Resultant Power Losses and Temperatures for the Proposed Topology

Switch	Losses	Temperatures (degree Fahrenheit)
S <sub>1</sub>	1.6	71.1
S <sub>2</sub>	1.2	70.8
S <sub>3</sub>	0.6	70.4
S <sub>4</sub>	1.5	71.0

Obtained losses and the temperatures at each of the switchcasings for the proposed topology are presented in Table 2. Table 3 lists the losses and temperatures for each switch present in the conventional topology.

**Table 3 Power Losses and Temperatures Recorded for the Conventional Topology**

Switch	Losses	Temperatures (degree Fahrenheit)
S <sub>1</sub>	0.99	70.7
S <sub>2</sub>	0.95	70.6
S <sub>3</sub>	0.73	70.5
S <sub>4</sub>	0.75	70.5
S <sub>5</sub>	2.02	71.4
S <sub>6</sub>	1.99	71.4

These simulation results can be validated mathematically, by using the following equation.

$$Temperature = (Ambient\ temperature) + (RJC + RTIM + RH) * (Losses) \quad (52)$$

When comparing the switching losses presented in Table III, it can be noted that similar temperatures were obtained, and only negligible differences were observed among the losses obtained across the switches.

## SIMULATION RESULTS

Considering  $V_s = 100V$ ,  $L_1 = L_2 = L_3 = 0.06mH$ ,  $C_1 = C_2 = C_3 = 0.0022F$ ,  $R_1 = R_2 = R_3 = 100\Omega$ ,  $V_{R1} = 55V$ ,  $V_{R2} = 30V$ , and  $V_{R3} = 15V$  as the parameters, the simulation of the proposed topology is analyzed using PSIM.

Simulation results obtained for the gating signals, output voltages, and regulating the output voltages for are shown in Fig. 6 and Fig. 7. Simulation results achieved are shown in the Fig. 8, Fig. 9, and Fig. 10. Fig. 8 shows the currents and voltages across inductor  $L_1$  and the output voltage  $V_{01}$ . Fig. 9, shows the current  $I_{L2}$  and voltages across inductor  $L_2$  and at the load  $R_2$ . Fig. 10 shows their corresponding simulation results. Fig. 12(a), shows the current  $I_{L3}$  and voltages across inductor  $L_3$  and at the load  $R_3$ .

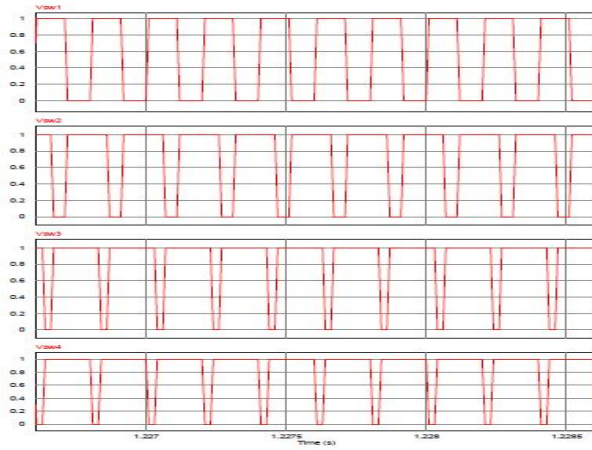


Fig. 6. Gating signal

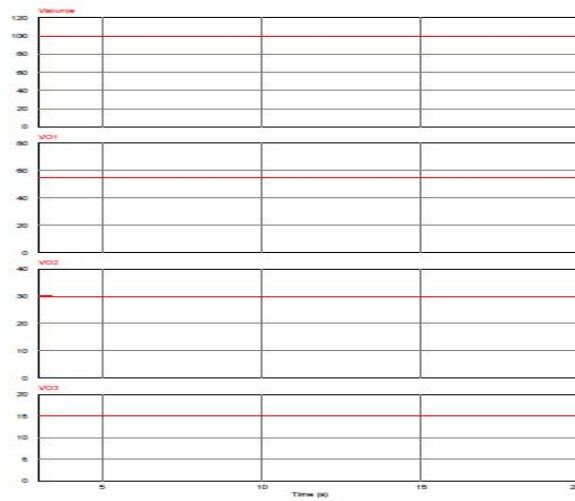


Fig. 7. Input and Output Voltages

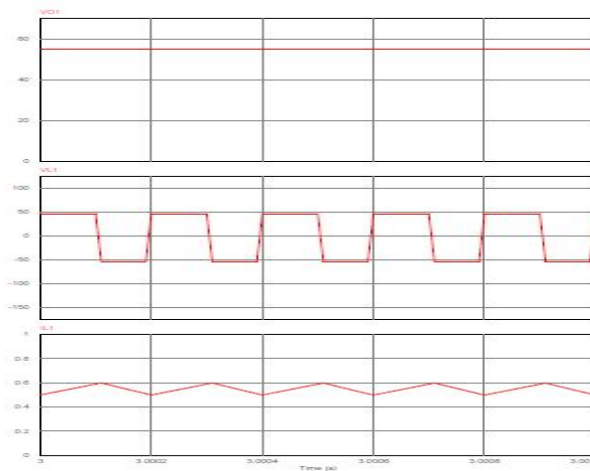


Fig. 8. output voltage  $V_{01}$ , Inductor voltage  $V_{L1}$ , and Inductor current  $I_{L1}$

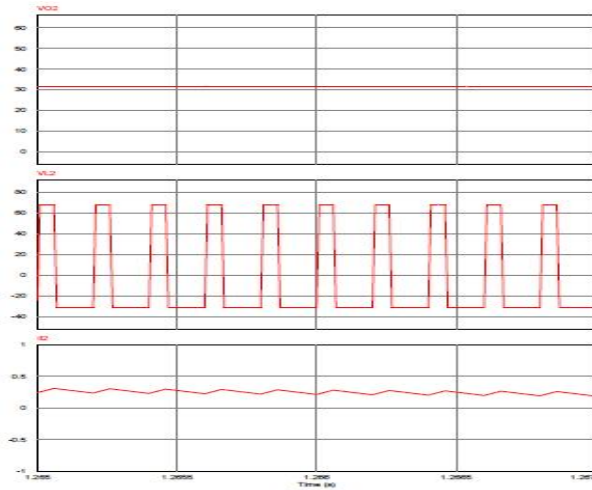


Fig. 9. output voltage  $V_{02}$ , Inductor voltage  $V_{L2}$ , and Inductor current  $I_{L2}$

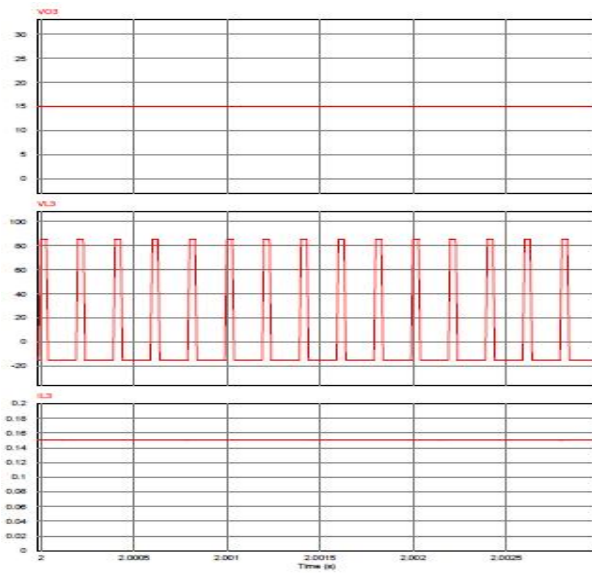


Fig. 10. Output voltage  $V_{03}$ , Inductor voltage  $V_{L3}$ , and Inductor current  $I_{L1}$

## CONCLUSION

This paper presents a novel single-input three-output DC-DC buck converter. The converter topology, operational modes, modulation technique, and design requirement have been studied. Although, the proposed converter needs superior current rating for switches, it decreases the number of switches required, and the number of driver circuits. The proposed converter also caters better power loss division among the switches. The proposed method is very advantageous from the economical point of view. It also reduces the size of the converter for same output with respect to conventional topology.



## REFERENCES

1. Ghodke, D., Chatterjee, K., Fernandes, B. Modified soft-switched three-phase three-level dc-dc converter for high-power applications having extended duty cycle range, *IEEE Trans. Ind. Electron.*, 2012;59(9): 3362–3372
2. Pahlevaninezhad, M., Drobnik, J., Jain, P., Bakhshai, A. A load adaptive control approach for a zero-voltage-switching dc-dc converter used for electric vehicles, *IEEE Trans. Ind. Electron.*, 2012; 59(2):920-933.
3. Yang, L.-S., Liang, T.-J. Analysis and implementation of a novel bidirectional dc-dc converter, *IEEE Trans. Ind. Electron.*, 2012; 59(1):422-434.
4. Lee, J.-Y., Jeong, Y.-S., Han, B.-M. An isolated dc-dc converter using high-frequency unregulated LLC resonant converter for fuel cell applications”, *IEEE Trans. Ind. Electron.*, 201; 58 (7):2926-2934.
5. Ouyang, Z., Zhang, Z., Thomsen, O.C., Andersen, M.A.E. Planar-integrated magnetics (PIM) module in hybrid bidirectional dc-dc converter for fuel cell application, *IEEE Trans. Power Electron.*, 2011; 26(11): 3254-3264.
6. Wang, L., Wang, Z., Li, H. Asymmetrical duty cycle control and decoupled power ow design of a three-port bidirectional dc-dc converter for fuel cell vehicle application, *IEEE Trans. Power Electron.* 2012; 27:891-904.
7. Nasiri, A., Nie, Z., Bekiarov, S.B., Emadi, A. An on-line ups system with power factor correction and electric isolation using BIFRED converter, *IEEE Trans. Power Electron.*, 2008; 55(2):722–730.
8. Zhang, Z., Ouyang, Z., Thomsen, O.C., Andersen, M.A.E. Analysis and design of a bi-directional isolated dc-dc converter for fuel cells and super capacitors hybrid system, *IEEE Trans. Power Electron.* 2012;27(2): 848-859.
9. Wu, H., Lu, J., Shi, W., Xing, Y. Non-isolated bidirectional dc-dc converters with negative-coupled inductor, *IEEE Trans. Power Electron.*, 2012;27(5):2231-2235.
10. Tan, N.M.L., Abe, T., Akagi, H. Design and performance of a bidirectional isolated dc-dc converter for a battery energy storage system, *IEEE Trans. Power Electron.*, 2012; 27(2): 1237- 1248.
11. Jin, K., Ruan, X., Yang, M., Xu, M. Power management for fuel-cell power system could start, *IEEE Trans. Power Electron.* 2009; 24(10): 2391-2395.

12. Shen, M., Peng, F.Z., Tolbert, L.M.: Multilevel dc-dc power conversion system with multiple dc sources, *IEEE Trans. Power Electron.*, 2008; 23(1): 420-426
13. Ni, L., Patterson, D.J., Hudgins, J.L. High power current sensorless bidirectional 16-phase interleaved dc-dc converter for hybrid vehicle application, *IEEE Trans. Power Electron.*, 2012; 27 (3):1141-1151.
14. Li, W., He, X. A family of isolated interleaved boost and buck converters with winding-cross-coupled inductors, *IEEE Trans. Power Electron.*, 2008; 23(5): 3164-3173
15. Belloni, E.B.M., Maloberti, F. On the design of singleinductor double-output dc-dc buck, boost and buck- boost converters. *15th IEEE Int. Conf. on Electronics, Circuits and Systems, ICECS 2008*, September, 2008;626-629
16. Rojas-Gonzalez, M., Torres, J., Sanchez- Sinencio, E., Kumar, P. An integrated dual-output buck converter based on sliding mode control. *IEEE Third Latin American Symp. Circuits and System*, 2012; 14.
17. Cavalcanti, M.C., da Silva, E., Boroyevich, D., Dong, W.,Jacobina, C.B. A feasible loss model for IGBT in soft-switching inverters. *Proc. IEEE PESC*, 2003;1845-1850
18. E. C. dos Santos Jr. Dual-output DC-DC Buck converters with bidirectional and unidirectional Characteristics, *IET Transactions on Power Electronics*, May2013; 6(5): 999–1009.
19. M. K. Reddy, C.Kalyani, M.Uthra and D.Elangovan: A small signal analysis of dc-dc boost converter, *Indian Journal of Science and Technology*, 2015.
20. S. Yang, K.Goto, Y. Imamura and M. Shoyama, Dynamic characteristics of bidirectional dc-dc converter using state-space averaging method,*INTELEC*, 2012.



**Dr.K.RAVI KUMAR**

He received B.Tech (EEE) and M.Tech (P.E) from the Jawaharlal Nehru Technological University Hyderabad in 1998 and 2005 respectively. He obtained his PhD degree in Electrical Engineering from NITWarangal under the guidance of Prof. M. Sydulu in 2016. Since 2001, He has been working as Associate Professor with the Electrical & Electronics Engineering department, Vasavi College of Engineering, Hyderabad. His interests include power system optimization, AI applications to power systems, Economic operation of power systems, power quality, power system stability, contingency analysis, smart grid, renewable energy systems and power electronic.



**M.SAI KUMAR**

He received B.Tech (EEE) from Gurunanak Institute of Technical Campus, Ibrahimpatnam, Rangareddy District. He pursuing his M.E (P.S.P.E) from Vasavi College of Engineering, Ibrahimbagh, Hyderabad. His interests include Power Electronics and power systems.

