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Survey On Don't Care Bit Filling Techniques For Low Power Testing

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ABSTRACT

One of the major problems in the field of VLSI testing is power consumption. Many techniques have been developed so far to generate the test patterns for both combinational and sequential circuits. The major issues in the generated test pattern is don't care bits. These don't care bits should be filled in appropriate manner to reduce the power consumption. Dynamic power dissipation is one of the major source of power consumption. It occurs during the logic switching of internal circuits. Proper filling of don't care bit is required to reduce the switching activity. This paper gives the detailed survey on don't care bit filling techniques.

KEYWORDS – Don't Care bit, Power Consumption, Test Patterns, Switching Activity

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I. INTRODUCTION

As a result of the emergence of new fabrication technologies, complexity of testing also increases. Chip production involves two steps. First one, fabricating an IC chip and second one simultaneous testing of those IC. Testing time for an IC is directly proportional to its input combination. Consider a 32 bit adder IC. Total number of test pattern combination to test a 32 bit adder is 2^{32}. The total number of test patterns will be 4294967296. If the time taken to apply a single test pattern is 1second, then time taken to test an IC will be approximately 236 years. When the circuit is a combinational circuit then we require 236 years. When a sequential circuit is to be tested then it takes many more years due to the flip-flop. A person who testes the IC will not have his lifetime sufficient to test single IC. This case is not possible in real time. So to avoid this problem we go for optimization (reduce the test data volume). Optimization technique helps in reducing the test patterns. Most of the EDA tools like Cadence and Synopsys used to optimize the test patterns [1]

The rest of the paper is organized as follows. The Impact of Test Power on X bits and don't care bit filling techniques are explained in section II. Experimental results are presented in section III. Concluding remarks are given in section IV.

II. SURVEY ON BIT FILLING TECHNIQUES

2.1 TEST POWER

It is very important to decrease the usage of power during testing. When the power is decreased then the test cost automatically decreases. If not then the costing of testing will be more than that of the price of the IC. Test patterns of sequential circuits consist of don't care bits. Several methods are used to fill the don't care bits of test vectors. The methods are Minimum transition filling, Column wise bit filling , 4m filling, Modified M filling , run of zeros followed by ones, run of one's followed by zeros, Runs of 'Zeros Followed by One' and ' Runs of Ones Followed by Zero etc..

The test pattern may also have don't care bits 'X' .These don't care bits should be replaced in a specific manner to reduce the power consumption. Choosing the value of the don't care should be in such a way that the switching should be minimum[2]. When the switching is reduced the power consumption directly decreases. In this paper we mainly use weighed transition metric. This is used for the estimation of average and peak power consumption[3].Test data has m patterns and the length of the patter is n bits. Each test patter denotes the jth bit in ith pattern. Weighed transitions metric for Tj the average test power Pavg and peak power Ppeak are estimated as per the formula

$$WTM_j = \sum_{i=1}^{n-1}(n-i) * (t_{j,i} \oplus t_{j,i+1})$$

$$P_{peak} = \max_{1 \le j \le m} WTM_j$$

$$P_{avg} = \frac{\sum_{j=1}^{m} WTM_j}{m}$$

2.2 METHODS OF FILLING DON'T CARE BITS:

All the test patterns generated has many don't care bits. These don't care bits when manipulated can enhance the data compression. So power can be reduced[4].

A. *Minimum transition bit filling technique*

In a minimum transition technique, consider a test vector matrix having 0, 1, X. Each row of the matrix corresponds to a test vector for the circuit. In this circuit x can be filled with either 0 or 1. Filling of X can be done randomly with 0 or 1. This can increase the chance of switching over. As the power factor should be reduced, the X should filled properly. In Minimum transition method all the X are filled with the same values. The values will be the previous value of the last X. Filling all the X in this method can minimizes the number of transitions when the test vector is scanned.

Eg) 1001XX0111XXX10

These don't cares when filled with Minimum transition we get 100111011111110.

B. *Column bit filling*[5]

In this technique the 'X' bits are filled column wise in accordance with the above value.

Eg) 1XXX

0XX1

1X1X

Then when Column bit filling is applied then we get

1111

0111

1111

C. *Run of zeros followed by ones*

In this technique all the X are just replaced by 0. This method is mainly used for codes like FDR or MFDR

Eg) 1001XX0110XXX10

When run of zeros followed by ones is applied then we get 100100011000010

D. *Run of one's follower by zeros*[6]

The symbols are made of runs of 1s followed by bit '0'. Here all Xs are replaced by 1s. So the runs of 1s will increase.

Eg) 1000XX0111XXX10

When run of one's followed by zeros is applied we get 100011011111110

E. Zeros Followed by One' and ' Runs of Ones Followed by Zero

This method is used in maximizing the run length. So all the X followed by 1 is replaced with 0 and all the X followed by 0 is replaced with 1.

Eg) 1001XX0110XXX10

These don't cares are filed as 100100011011110

F. 4m filling

This method divides the data by group of 4 bits . Then any of these methods can be used in filling.

Eg) X0X000X1000111111110100010011 01X111000011011X1XX1X1XX1

Splitting the data in to 4 and filed values gives

1010010011111111111010001001101111100001101111111111111

G. Modified 4m Filling [7]

The Modified 4m filling initially checks the first bit of every test pattern; if the test pattern coming with leading X bit, then it checks for immediate preceding specified bit appears in the test pattern. Once the specified bit is identified, X-bits are filled with the same specified bit which is similar to adjacent filling. Modified 4m filling continuously counts X-bit till non X bit. Fill the non X bit with X bit.

Eg) X0X000X1000111111110100010011 01X111000011011X1XX1X1XX1

These don't cares are filed as

0000000100011111111010001001101111100001101111111111111

III. EXPERIMENT AND RESULT

This paper describes varies processes which reduces the weighted transition using Minimum transition filling, Column wise bit filling , 4m filling, Modified 4M filling , run of zeros followed by ones, run of one's followed by zeros, Runs of 'Zeros Followed by One' and ' Runs of Ones Followed by Zero . Table 1 and Table 2 shows the peak power and Average power estimated for the ISCAS Benchmark Sequential circuits for the above filling methods

Table -1: Peak Power Dissipation of ISCAS Benchmark sequential circuits

ISCAS Circuit	Peak Power					
	A	B	C	D	F	G
S5378	12085	12375	11732	11522	10908	10042
S9234	15395	15640	14092	14103	15143	12653
S13207	110129	126820	94879	94886	76140	81122
S15850	84360	88794	70875	70894	62269	63632
S38417	514716	539019	437884	437935	304948	356910
S38584	530464	533975	481158	481171	528835	483002

Table -2: Average Power Dissipation of ISCAS Benchmark sequential circuits

ISCAS Circuit	Average Power					
	A	B	C	D	F	G
S5378	4300	4087	3254	3526	3796	2755
S9234	6706	6521	4002	4022	5511	3849
S13207	12318	1453	8073	7887	6710	8493
S15850	19448	25636	13611	13659	14209	14095
S38417	194843	193140	118100	118080	142560	113323
S38584	133320	142220	86135	86305	117550	89659

IV.CONCLUSION

For any chip, Power is calculated by $P \alpha CV^2f$. It means the switching activity is directly proportional to power dissipation. This paper gives the latest filling techniques of 'X' Bits to reduce the switching activity. This test vector is generated by Automatic test pattern generation method. It is done by replacing don't care bit to a defined bit for different existing methods also average power and peak power are discussed in this paper.

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