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### **Reduction of THD Using Three and Five Level Diode Clamped Multilevel Inverter**

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#### **ABSTRACT**

This paper presents a five level and three level diode clamped multilevel inverter topology which can be used for low medium power industrial applications. The topology of five level and three level diode clamped multilevel inverter is tested using MATLAB. Circuit operation is presented, simulated & Total Harmonic Distortion is analyzed. To obtain sinusoidal output voltage with low harmonics, multicarrier PWM technique is used for diode clamped multilevel inverter.

**KEYWORDS:** Diode clamped multilevel inverter, PWM technique

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## INTRODUCTION

The multi level inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations because they have many advantages, such as low voltage stress on power switches, low harmonic and EMI output. Another name for diode clamped multilevel inverter is neutral point clamped (NPC) inverter. The main concept of diode clamped inverter is to use diodes and provides more voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thus reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. This problem can be eliminated by increasing the switches, diodes and capacitors. This type of inverters provides high efficiency because the fundamental frequency used for all the switching devices.

## DRIVE SYSTEM DESCRIPTION

In the conventional method ordinary PWM method is used. Here switching frequency causes more amount of switching loss. These problems are corrected using three phase diode clamped multilevel inverter. Here switching losses are reduced when compared to the conventional technique.

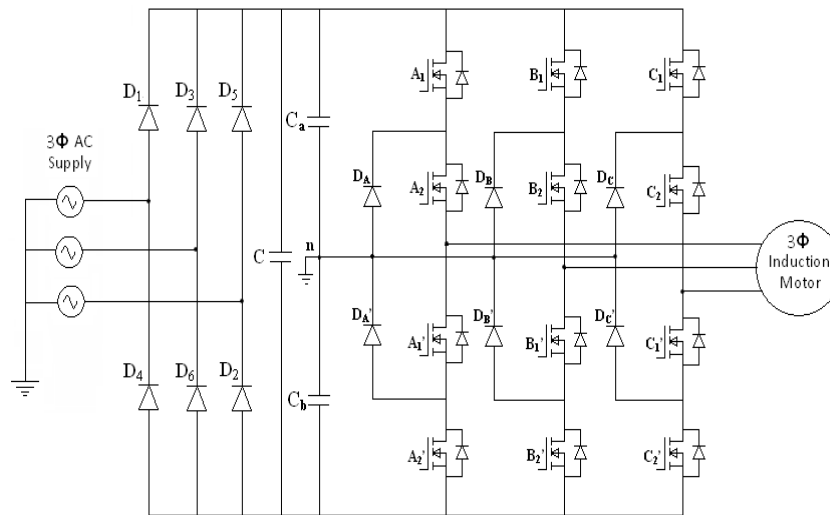


Figure.1: Multilevel inverter based drive circuit

## PRINCIPLE OF OPERATION

To produce an output voltage in staircase shape, consider one leg of a three-level inverter, as shown in Figure.2. The steps to produce the three-level voltages are as follows.

1. For an output voltage level  $V_{ao} = V_{dc}$ , turn on all upper leg switches  $A_1$  and  $A_2$ .
2. For an output voltage level  $V_{ao} = V_{dc}/2$ , turn on one upper switch  $A_2$  and one lower switch  $A_1'$ .
3. For an output voltage level  $V_{ao} = 0$ , turn on all lower leg switches  $A_1'$  and  $A_2'$ .

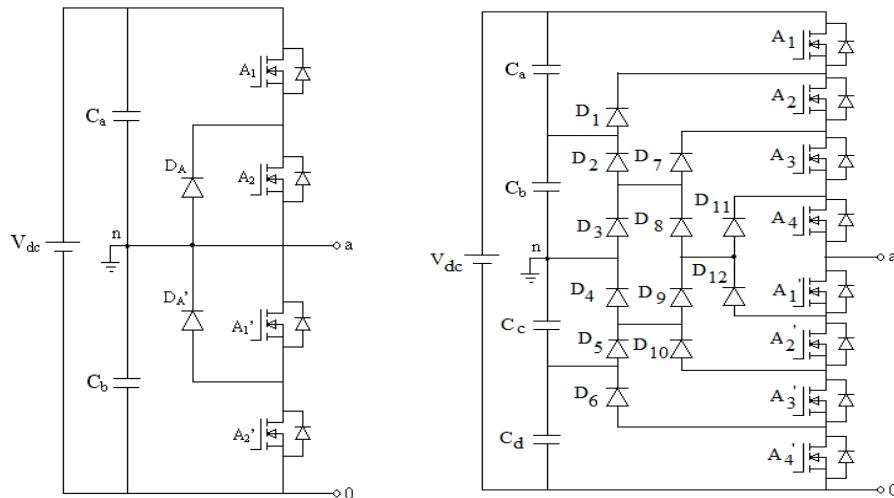


Figure.2: One Leg of a Three Level & Five Level Inverter

Table.1. shows the voltage levels for three level inverter and their corresponding switch states. Switch is on means state condition is 1, 0 means the switch is off. There are two opposite switch pairs in each phase.

Table 1: Voltage level for three level inverter and their Switching states

Output $v_{ao}$	Switch states			
	$A_1$	$A_1'$	$A_2$	$A_2'$
$V_{dc}$	1	1	0	0
$V_{dc}/2$	0	1	1	0
0	0	0	1	1

To produce an output voltage in staircase shape, consider one leg of a five-level inverter, as shown in Figure.2. The steps to produce the five-level voltages are as follows.

1. For voltage level  $V_{ao} = V_{dc}$ , turn on all upper switches  $A_1 - A_4$ .
2. For voltage level  $V_{ao} = 3V_{dc}/4$ , turn on three upper switches  $A_2 - A_4$  and one lower leg switch  $A_1'$ .
3. For voltage level  $V_{ao} = V_{dc}/2$ , turn on two upper switches  $A_3$  and  $A_4$  and two lower switches  $A_1'$  and  $A_2'$ .
4. For voltage level  $V_{ao} = V_{dc}/4$ , turn on one upper switch and three lower switches  $A_1' - A_3'$ .
5. For voltage level  $V_{ao} = 0$ , turn on all lower switches  $A_1' - A_4'$ .

Four opposite switch pairs exist in each phase. The opposite switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four opposite pairs are  $(A_1, A_1')$ ,  $(A_2, A_2')$ ,  $(A_3, A_3')$ , and  $(A_4, A_4')$ .

Table 2: Voltage level for five level inverter and their Switching states

Output $v_{ao}$	Switch states							
	$A_1$	$A_2$	$A_3$	$A_4$	$A_1'$	$A_2'$	$A_3'$	$A_4'$
$V_{dc}$	1	1	1	1	0	0	0	0
$3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_{dc}/2$	0	0	1	1	1	1	0	0
$V_{dc}/4$	0	0	0	1	1	1	1	0
0	0	0	0	0	1	1	1	1

## MODULATION STRATEGY

This paper mainly focuses on multicarrier PWM method. This method is easy and more flexible than SVM methods. Multicarrier PWM method can be categorized into three groups:

- Alternative Phase Opposition Disposition (APOD)
- Phase Opposition Disposition (POD)
- In-Phase Disposition (PD)

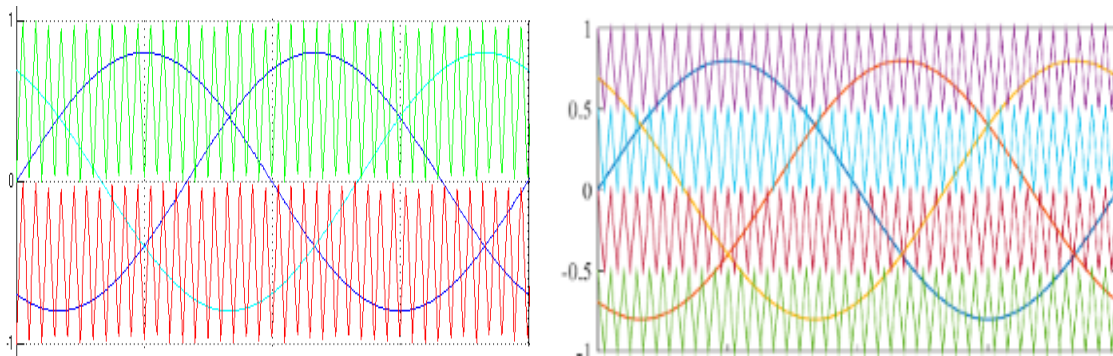


Figure.3: In-Phase Disposition Technique for 3-Level & 5-Level Multilevel Inverters

Figure.3. demonstrates the sine-triangle method for a three-level & five level inverters. Therein, the modulation signal is compared with N-1 triangle waveforms.

## SIMULATED CIRCUITS AND WAVEFORMS

The triggering circuit is formulated based on the three phase sinusoidal modulation waves,  $V_a$ ,  $V_b$ , and  $V_c$ . Three sine wave sources have been obtained with same frequency and amplitude but displaced  $120^\circ$  out of the phase with each others. For carriers wave sources block parameters, the time values of each carrier waves are set to  $[0, (1/2000)*1/2, 1/2000]$  while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the MOSFET switches.

Figure.4. shows the waveform of sine-triangle intersection. Two carriers together with sine wave have been used to obtain SPWM control.

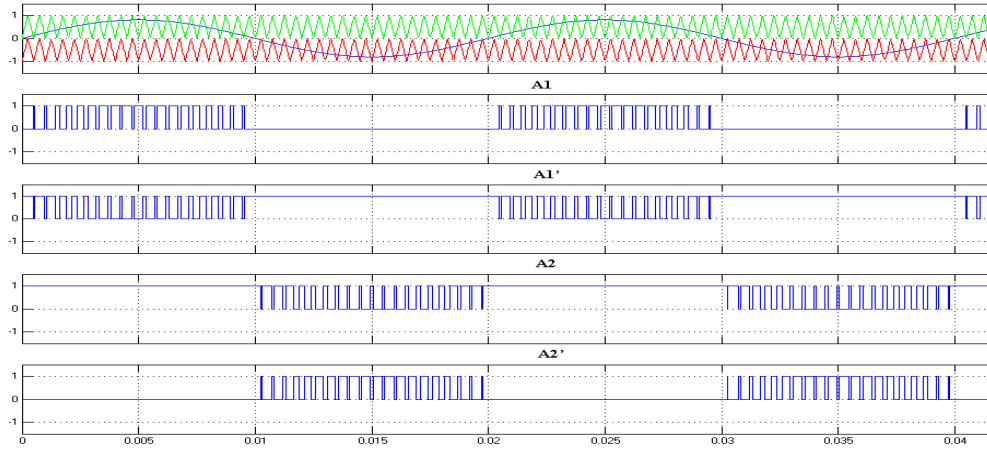


Figure.4: Gate Pulses for Leg A Switches.

Simulated model for entire circuit is shown in Figure.5.

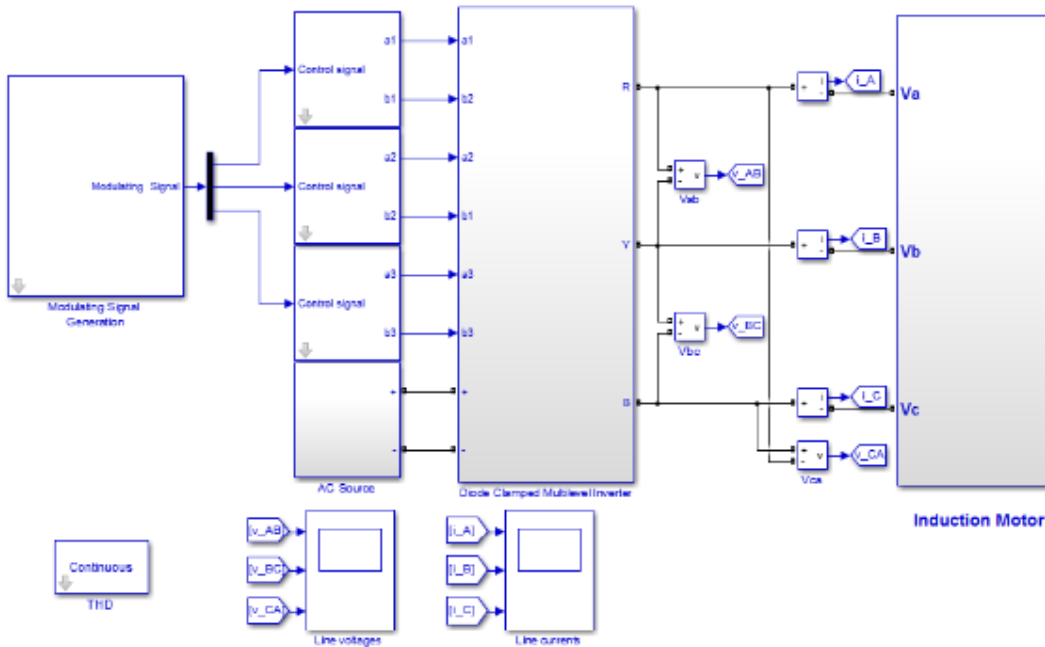


Figure.5: Simulated Circuit

Output voltage waveform for three level inverter is shown in Figure.6.

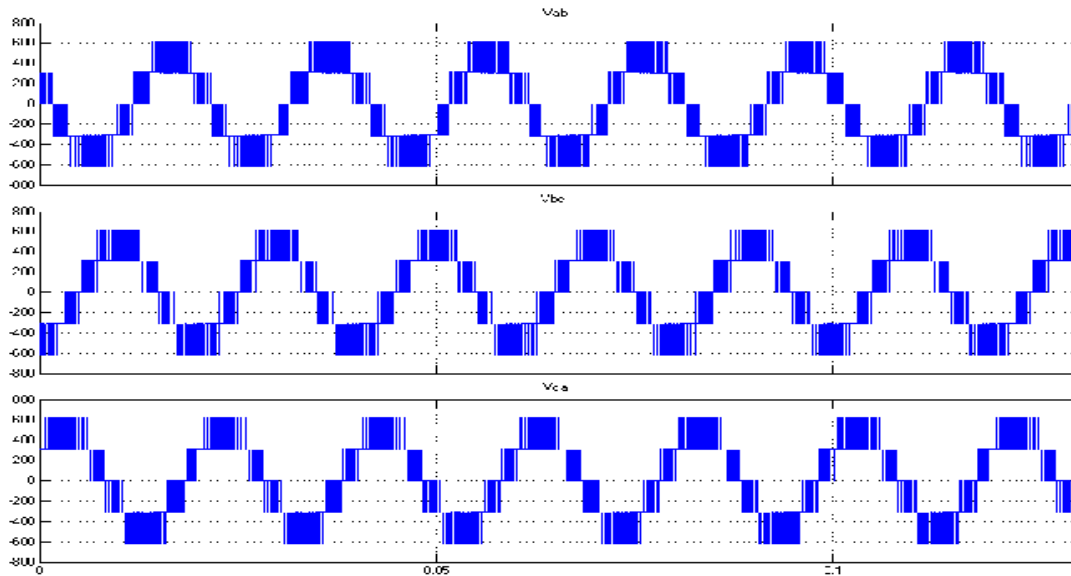


Figure.6: Output Line-Line Voltage for 3-Level Inverter

The FFT plot of the output voltage for three level inverter is shown in Figure.7. The plot shows that the harmonic content present in the output voltage is low.

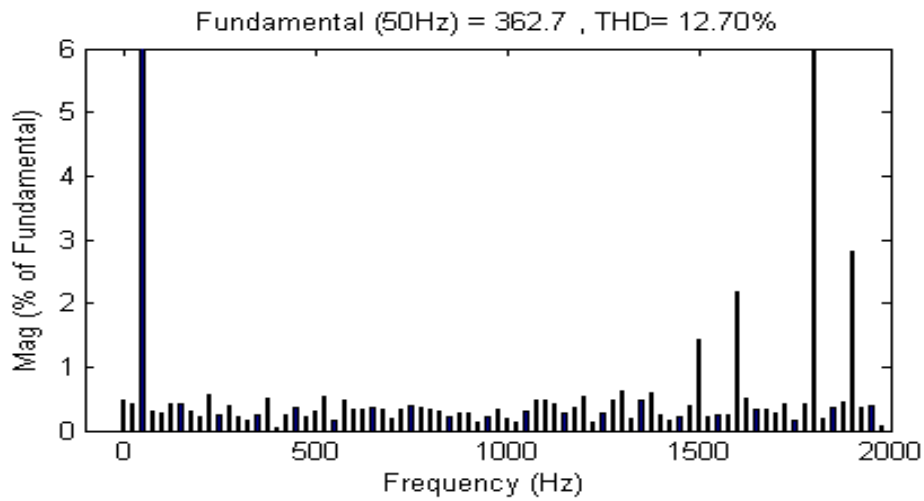


Figure.7: FFT for 3-Level Inverter

Output voltage waveform for five level inverter is shown in Figure.8.

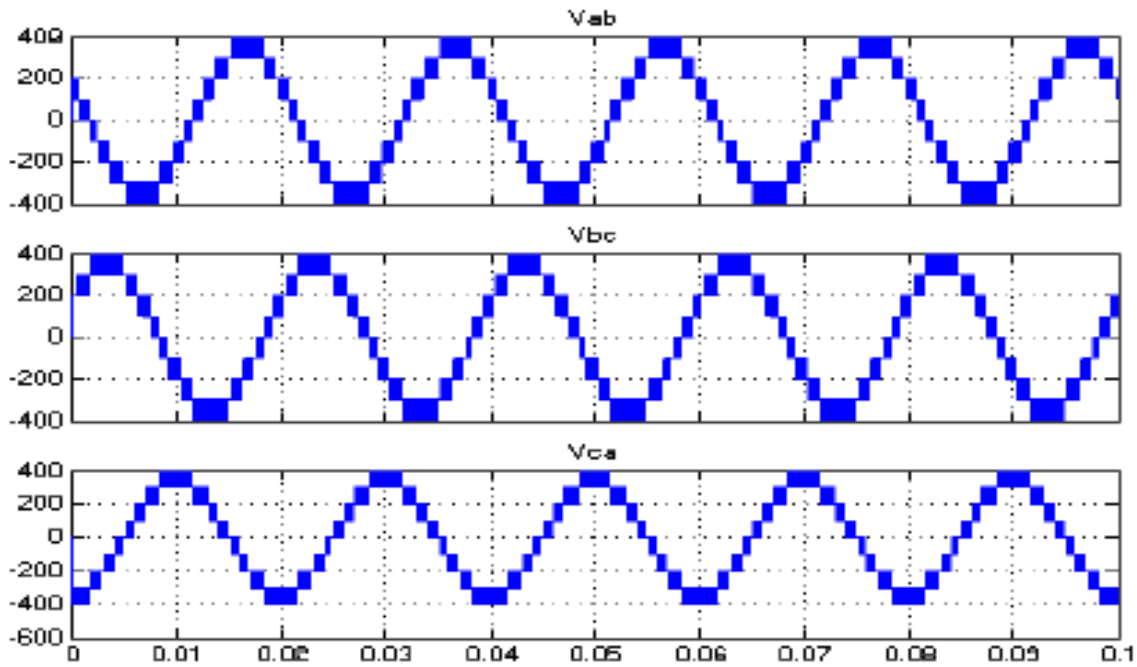


Figure.8: Output Line-Line Voltage for 5-Level Inverter

The FFT plot of the output voltage for five level inverter is shown in Figure.9. The plot shows that the harmonic content present in the output voltage is very low compared to three level inverter.

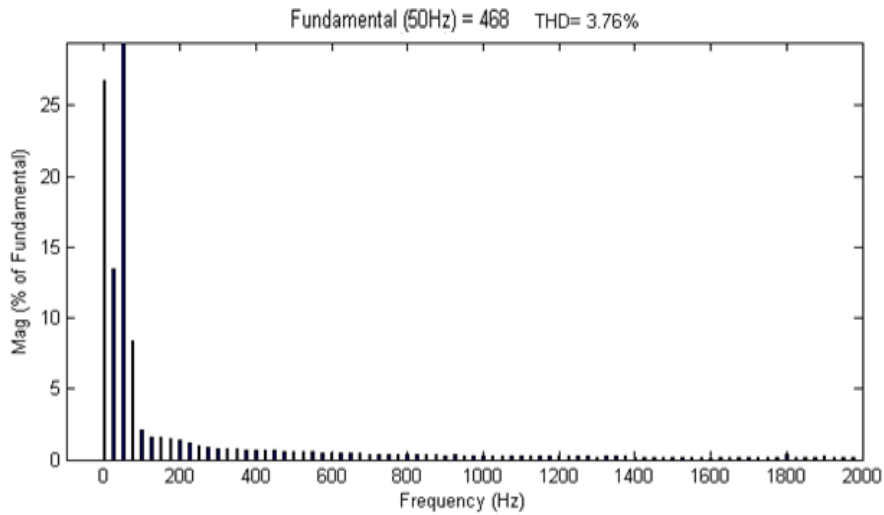


Figure.9: FFT for 5-Level Inverter

Table 3: Reduction of THD by varying inverter level

Number of levels	THD (%)
Three level	12.70
Five level	3.76

## CONCLUSION

An In-phase disposition technique is proposed for three-level and five-level NPC inverters. The main feature of the modulation scheme is to eliminate the harmonics in the inverter output

voltages. To assist the analysis and design of the classical scheme, the mechanism of the THD reduction with increase in level of inverter employing in-phase disposition technique is discussed. The THD of the inverter output voltage produced by the three and five levels are compared.

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