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A Novel Sleep Transistor Insertion Methodology for Leakage Power Optimization in Nanometer CMOS Circuits

Zaddaraju*, P.Prasanna Murali Krishnna and P.Srinivasulu

Department of ECE, Dr.S.G.I.E.T, Markapur, Andhra Pradesh, India

ABSTRACT

As technology scales into the nanometer regime ground bounce noise and noise immunity are becoming important metric of comparable importance to leakage current, active power, delay and area for the analysis and design of complex arithmetic logic circuits. In this paper, low leakage 1bit full adder cells are proposed for mobile applications with low ground bounce noise and a novel technique has been introduced with improved staggered phase damping technique for further reduction in the peak of ground bounce noise. Noise immunity has been carefully considered since the significant threshold current of the low threshold voltage transition becomes more susceptible to noise. We introduced a new transistor resizing approach for 1bit full adder cells to determine the optimal sleep transistor size which reduce the leakage power and ground bounce noise. The simulation results depicts that the proposed design also leads to efficient 1bit full adder cells in terms of standby leakage power, active power, ground bounce noise and noise margin. We have performed simulations using Cadence Specter 90nm standard CMOS technology at room temperature with supply voltage of 1V.

KEYWORDS—Low leakage power; Noise Margin; Ground bounce noise; Optimal Sleep transistor and Adder cell.

Corresponding Author-

Zaddaraju

M.Tech (DECS) Student, *Department of ECE,*
Dr.S.G.I.E.T, Markapur, Andhra Pradesh, India
Email: psrinivas.vlsi@gmail.com

I. INTRODUCTION

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition [1,2]. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is not related to ensuring correct circuit operation, but is related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call). When an electronic device such as a mobile phone is in standby mode, certain portions of the Circuitries within the electronic device, which are active when the phone is in talk mode, are shut down. These circuits, however, still have leakage currents running through them, even though they have been de-activated. Even if the leakage current is much smaller than the normal operating current of the circuit. The leakage current depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. This is why building low leakage adder cells for mobile applications are of great interest[4].

To summarize, some performance criteria are considered in the design and evaluation of adder cells, such as leakage power, active power, ground bounce noise, area, noise margin and robustness with respect to voltage and transistor scaling as well as varying process and compatibility with surrounding circuitries.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate [5,6]. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30xincrease in gate leakage [7,8]. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation [9]. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques to reduce leakage power [10].

Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground) [11,12, 13, 14]. This device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance [15, 16 ,17, 18] and further peak of ground bounce noise is possible with proposed novel technique with improved staggered phase damping technique.

This paper focuses on reducing sub threshold leakage power consumption and ground bounce noise.

The remainder of this paper is organized as follows. In section II, proposed nano- CMOS full adder circuits, and its equivalent circuits are discussed. In section III, the performance analysis and simulation results of conventional CMOS full adder cell and proposed circuits are explained. Then the paper is summarized in section IV.

II. PROPOSED FULL ADDER CIRCUITS

Recently, power dissipation has become an important concern and considerable emphasis is placed on understanding the sources of power and approaches to dealing with power dissipation [3].

Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous when we implement by the pass transistor logic [4]. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability [4,13].

Fig. 1 shows the conventional CMOS 28 transistor adder [12]. This is considered as a Base case throughout this paper. All comparisons are done with Base case.

The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs.

Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays a key role in static CMOS style. It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters. This ratio does not give best results with respect to noise margin and standby leakage power when it is simulated in 90nm process. Modified adder circuits with sizing are proposed in Design1 and Design2 targeting the noise

margin, and ground bounce noise.

Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. Further, the peak of ground bounce noise is achieved with a proposed novel technique.

Modified sizings are shown in Fig. 2 and Fig. 5 respectively. The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and gives W/L ratio of 1.2. The W/L ratio of NMOS is fixed at 1.2 and W/L of PMOS is 3.8 which is 3.1 times that of NMOS in Design1. The sizing of each block is based on the following assumption.

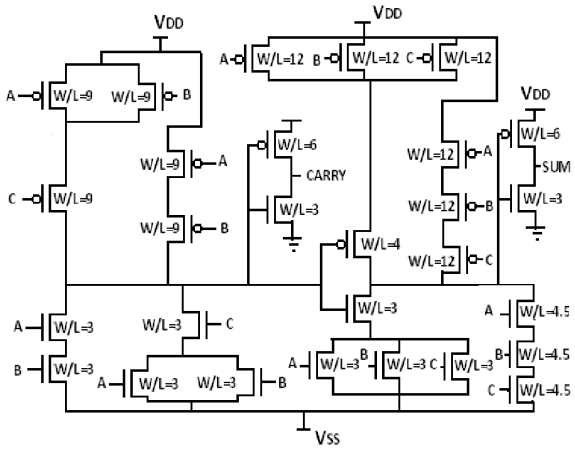

Figure 1. Conventional CMOS full adder.

Base case is considered as individual block as shown in Fig. 3. Each block has been treated as an equivalent inverter. The same inverter ratio is maintained on each block. These sizing will reduce the standby leakage current greatly because subthreshold current is directly propotional to the Width/Length ratio of transistor. On the other hand, these reduced sizes will reduce the area occupied by the circuit. This will reduce the silicon chip area and obviously there will be a reduction in the cost.

Modified adder circuit i.e Design2 shown in Fig. 5, the W/L ratio of PMOS is 1.5 times that of W/L ratio of NMOS and each block has been treated as an equivalent inverter. The same inverter size has been maintained on each block as shown in the Fig. 4. The goal of this design is to reduce the standby leakage power. Further compared to the Base case and Design1 and ground bounce noise produced when a circuit is connected to sleep transistor. However, there will be a slight variation on the noise margin levels and is almost equal to the Base case.

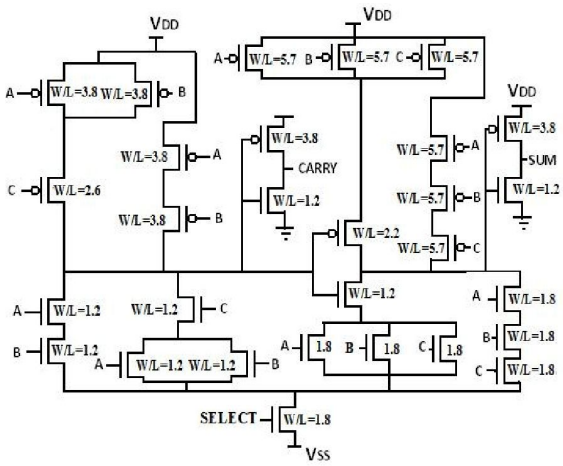

Figure 2. Proposed full adder (Design1) circuit with sleep transistor.

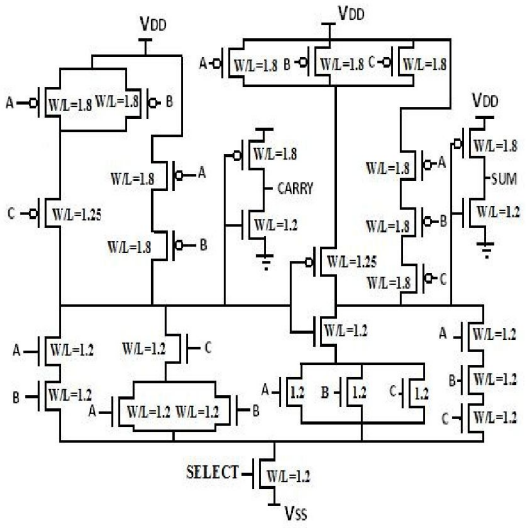

Figure 3. Equivalent circuit for Design1

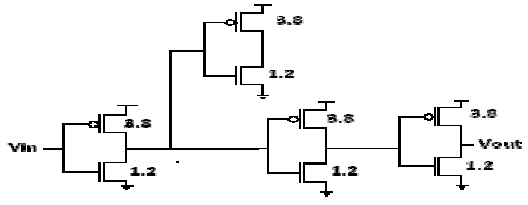

Figure 4. Equivalent circuit for Design2.

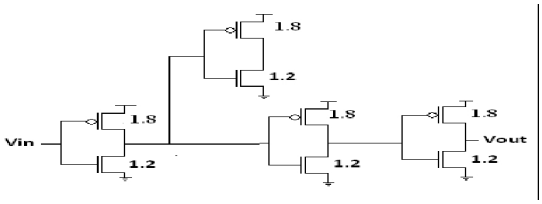

Figure 5. Proposed 1 bit full adder (Design2) circuit with sleep transistor

III. PERFORMANCE ANALYSIS AND SIMULATION RESULTS

We have performed post layout simulations using cadence-spectre simulator and the technology being employed for simulation is 90nm.

A. Noise Margin

The noise margin is measured by the voltage transfer characteristic of a circuit. Sweep waveform varying from 0 to 1 with an increment of 0.001 volts has been given to one of the input named as S and different DC values are given to remaining inputs shown in the Table I. The values of $V_{TH,}$ $V_{IL,}$ V_{IH} can be calculated by the obtained DC transfer characteristic of the circuit. As illustrated in the Table I and II, noise margin of Design1 is comparable to the Base case and switching threshold voltage levels are almost approaches to V_{DD} / 2 i.e.0.5 and noise margin levels of Design2 are comparable to the Base case.

B. Active power

The power dissipated by the circuit when the circuit is in active state. Active power is measured by giving input vectors and calculating the average power dissipation during this time. Considered simulation time to calculate active power is 50ns. Input vectors have been given in such a way that it covers almost all input vector combinations. The same vectors and simulation time has been given to Base case to compare the results. This active power includes dynamic power as well as the static power so it is being named as an active power.

TABLE I. Noise Margins For Base Case And Design1

Input Vector	Base case			Design1		
	VTH (V)	NM_L (V)	NM_H (V)	VTH (V)	NM_L (V)	NM_H (V)
S00	0.53	0.50	0.45	0.47	0.44	0.50
S01	0.51	0.50	0.48	0.48	0.47	0.51
S10	0.52	0.51	0.46	0.52	0.51	0.48
S11	0.53	0.50	0.44	0.53	0.50	0.44
0S0	0.51	0.48	0.46	0.48	0.46	0.49
0S1	0.49	0.48	0.49	0.50	0.49	0.49
1S0	0.51	0.49	0.46	0.49	0.49	0.50
1S1	0.51	0.49	0.46	0.52	0.49	0.50
00S	0.50	0.47	0.47	0.50	0.48	0.47
01S	0.47	0.45	0.52	0.48	0.47	0.52
10S	0.50	0.47	0.47	0.48	0.47	0.52
11S	0.50	0.47	0.47	0.50	0.47	0.47

As shown in the Table. III, both Design1 and Design2 active power is greatly reduced compared to the Base case. This reduction is almost 40.49% and 63.87% in case of Design1 and Design2 respectively compared to the Base case.

TABLE II. Noise Margins For Base Case And Design2

Input Vector	Base case			Design2		
	VTH (V)	NM_L (V)	NM_H (V)	VTH (V)	NM_L (V)	NM_H (V)
S00	0.53	0.50	0.45	0.47	0.44	0.49
S01	0.51	0.50	0.48	0.44	0.45	0.57
S10	0.52	0.51	0.46	0.45	0.47	0.56
S11	0.53	0.50	0.44	0.52	0.54	0.52
0S0	0.51	0.48	0.46	0.46	0.48	0.59
0S1	0.49	0.48	0.49	0.41	0.40	0.58
1S0	0.51	0.49	0.46	0.43	0.42	0.56
1S1	0.51	0.49	0.46	0.49	0.47	0.47
00S	0.50	0.47	0.47	0.43	0.47	0.60
01S	0.47	0.45	0.52	0.41	0.40	0.58
10S	0.50	0.47	0.47	0.41	0.41	0.42
11S	0.50	0.47	0.47	0.48	0.51	0.55

TABLE III.

ACTIVE POWER DISSIPATION OF 1-BIT FULL ADDER CELLS

Design name	Base case	Design1	Design2
Active power(µW)	3.488	2.076	1.261

TABLE IV.

AREA OF 1 BIT-FULL ADDER CELLS

Design name	Base case	Design1	Design2
Area (μm^2)	1.75	0.78	0.49

C. Standby leakage Power

Standby leakage power is measured when the circuit is in standby mode. Sleep transistor is connected to the pull down network of 1 bit full adder circuit. Sleep transistor is off by asserting an input 0V. For simplicity, size of a sleep transistor is equal to the size of largest transistor in the network (pull up or pull-down) connected to the sleep transistor. The sleep transistor size in Design1 and Design2 is reduced due to the resizing of the adder cells in proposed circuit. Standby leakage power is measured by giving different input combinations to the circuit. Standby leakage is greatly reduced in both Design1 and Design2 as shown in Fig. 9. In case of Design1 reduction in standby power is about 82% and in Design2 it is about 84% for all input combinations.

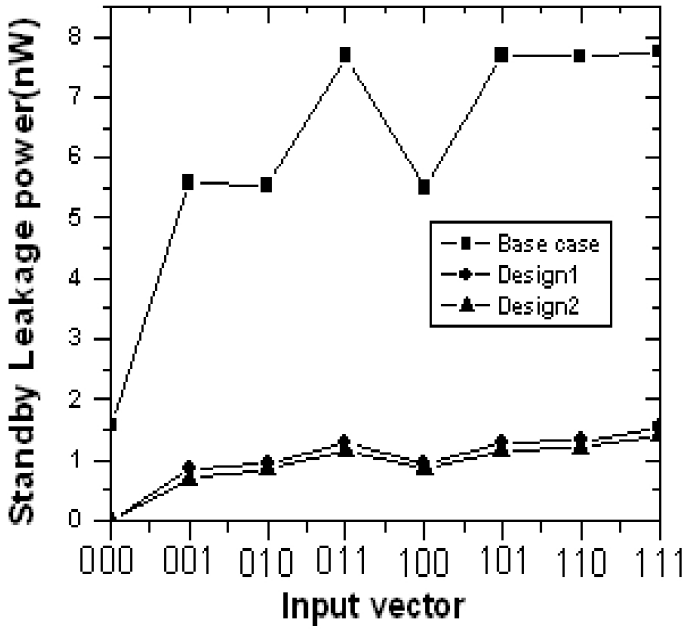

Figure 9. Comparison of standby leakage power with different input combinations of three designs.

D. Area

The layouts are used to calculate the areas of proposed designs. The parasitics have been considered in the designs. Layouts (90nm) of proposed full adder circuits (Design1) and (Design 2) are shown in Fig. 10 and Fig.11. Area is reduced 55.43% and 72% in Design1 and Design2 respectively comparing to the Base case and is depicted in Table. IV.

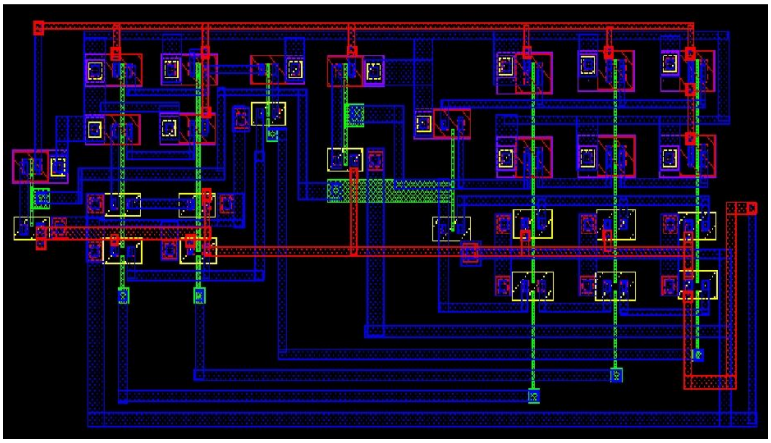

Figure 10. Layout of proposed full adder circuit (Design1) with 90nm technology

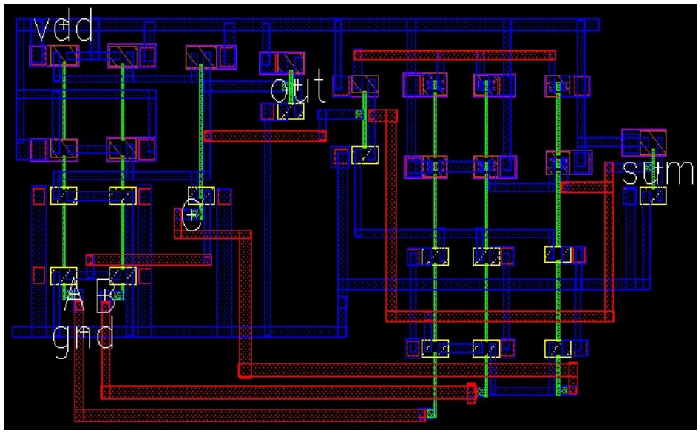

Figure 11. Layout of proposed full adder circuit(Design2) with 90nm technology .

E. Ground bounce noise reduction

During the power mode transition, an instantaneous charge current passes through the sleep transistor, which is operating in its saturation region, and creates current surges elsewhere, Because of the self-inductance of the off-chip bonding wires and the parasitic inductance inherent to the on-chip power rails, these surges result in voltage fluctuations in the power rails. If the magnitude of the voltage surge or circuit may erroneously latch to the wrong value or switch at the wrong time.

Inductive noise, also known as simultaneous switching noise, is phenomenon that has been traditionally associated with input/output buffers and internal circuitry. The noise immunity of a

circuit decreases as its supply voltage is reduced such as power gating to address the problem of ground bounce in low-voltage CMOS circuits. The ground bounce model which is used in our simulation is shown in Fig.12. Ground bounce noise is reduced in both Design1 and Design2 as compared to the Base case and is shown in Fig.13.

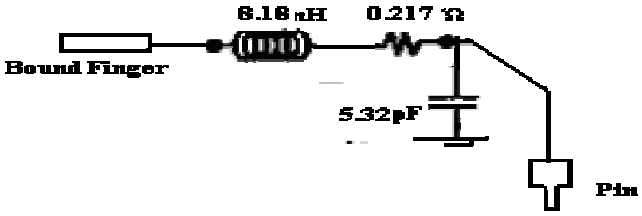

Figure 12. DIP -40 package pin ground bounce noise model [11].

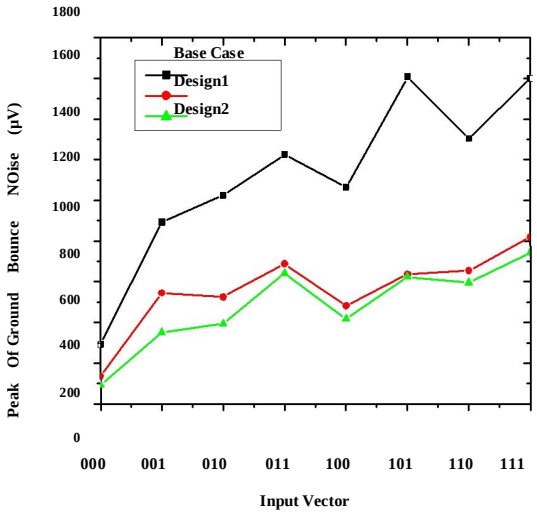

Figure 13. Peak of ground bounce noise comparison with proposed and conventional power gating technique (Base case, Design1, Design2).

F. Improved Ground bounce noise reduction

During last one decade various alternatives and improvements of conventional power gating has been proposed to reduce the ground bounce noise during mode transition. In staggered Phase Damping technique[15] during standby-to-active power mode transition, staggered-phase damping delays the activation time of one of the two sleep transistors relative to the activation time of the other one by a time that is equal to half the resonant oscillation period. As a result, noise cancellation occurs once the second sleep transistor turns on due to phase shift between the noise induced by the second sleep transistor hence reduction in settling time. But it is not very effective in reducing the

peak noise due to the initial spike. And in another scheme [17], there will be a two stage procedure. In first stage sleep transistor working as diode by turn on the control transistor which is connected across the drain and gate of the sleep transistor. Due to this drain to source current of the sleep transistor drops in a quadratic manner. This reduces the voltage fluctuation on the ground and power net and it also reduces the circuit wakeup time. In second stage control transistor is off so that sleep transistor works normally. This method is not effective to suppress the overall fluctuations in the ground bounce noise. Therefore, the technique must be adopted to reduce both peak of ground bounce noise and reducing the overall fluctuations in the ground bounce noise. The idea is to combine both the above techniques to further reducing the peak of ground bounce noise and overall power mode transition noise in the proposed technique.

Figure 14 shows the proposed scheme for peak of ground bounce noise reduction in mode transition. One bit full adders (Base Case, Design1, design2) have been taken to apply the proposed technique. One-bit full adder considered as two cascaded blocks i.e. carry generation block and sum generation block. Separate sleep transistors are added at the bottom of the blocks. The proposed technique works as follows. The applied signals are shown in this Fig.15. For carry part, during stage1 transmission gate is off by giving proper enable signals and at the same time control transistor is turned on to make the sleep transistor working as a diode. The stored charge in carry generation block is discharged through sleep transistor. The drain current of the ST1 during the this stage is as (1).

$$I_d=\mu_n C_{ox}\ (W/L)[(V_{GS}-V_{DS})V_{DS}-V_{DS}^2/2] \qquad (1)$$

Since the drain-to-source voltage of the control transistor (CT1) is zero, which makes $V_{DS}=V_{GS}$, the current Id goes through ST1 can be written as (2)

$$I_d=\mu_n C_{ox}\ (W/L)[(V_{DS}^2/2 -V_{th}V_{DS})] \qquad (2)$$

As the voltage level of virtual ground drops, VDS over the ST1 drops and this makes the drain to source current of the sleep transistor (ST1) I_D drops quadratic manner. The dropping Id decreases the voltage fluctuation on the ground and power net. And same signals are applied to sum generation part also but with duration of half of the oscillation period. As a result, noise cancellation occurs once the second sleep transistor (ST2) turns on due to phase shift between the noise induced by the second sleep transistor hence reduction in peak of ground bounce noise shown in Fig. 16.

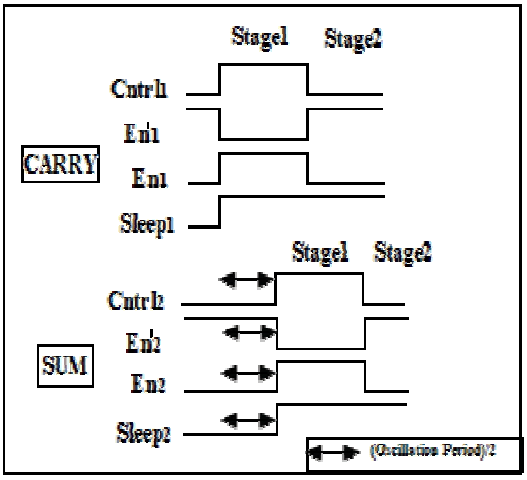

Figure 14. Proposed novel technique for ground bounce noise reduction.

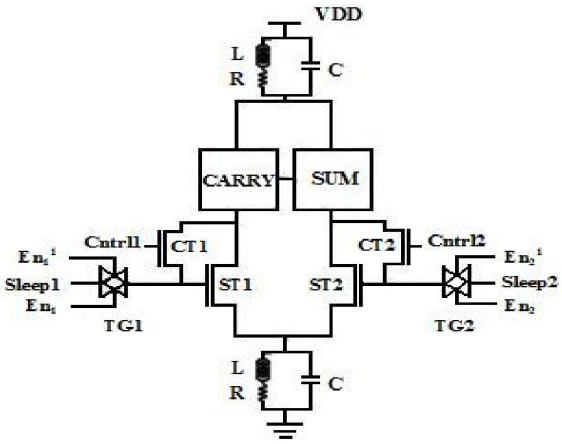

Figure 15. Applied signals to the proposed technique.

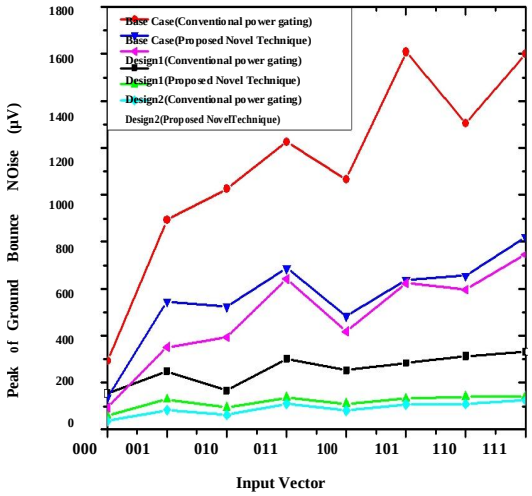

Figure 16. Peak of ground bounce noise comparison with proposed and conventional power gating technique (Base case, Design1, Design2).

IV.CONCLUSION

In this paper, low leakage 1 bit full adder cells are proposed for mobile applications with low ground bounce noise. Noise immunity has been carefully considered since significant threshold current of the low threshold voltage transition becomes more susceptible to noise. By using the proposed technique leakage power is reduced by 82 %(Design1), 84% (Design2) in comparison to the conventional adder cell (Base case). Ground bounce noise is reduced about 1.5 times and 3 times in Design1 and Design2 respectively compared to Base case. Further, using the proposed Novel technique the ground bounce noise is reduced to about 4.5 times in three designs (Base Case, Design1, Design2) compared to without applying the technique. Area is reduced by 55.4% in (Design1), 72% (Design2) in comparison to the Base case. Active power reduction is reduced by 40.48% (Design1), 63.38% (Design2) in comparison to Base case. Noise immunity of proposed full adder cells are comparable to the conventional adder cell (Base case). The proposed novel technique has been introduced with improved staggered phase damping technique for further reduction in the peak of ground bounce noise and overall power mode transition noise **.** The proposed 1-bit full adder cells are designed with 90nm technology and operated with 1V supply voltage.

V.REFERENCES

1. Radu Zlatanovici, Sean Kao, Borivoje Nikolic, “Energy-Delay of Optimization 64-Bit Carry-Lookahead Adders With a 240ps 90nm CMOS Design Example,” *IEEE J. Solid State circuits*, Feb. 2009; 44(2): 569-583.
2. K.Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, N. Dadkhai, “Low-Power and High-Performance 1-bit CMOS Full Adder Cell,” *Journal of Computers*, Academy Press, Feb. 2008;3(2).
3. Rabaey J. M., A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits, A Design Perspective*, 2nd Prentice Hall, Englewood Cliffs, NJ, 2002.
4. Pren R. Zimmermann, W. Fichtner, “Low-power logic styles: CMOS versus pass-transistor logic,” *IEEE J. Solid- State Circuits*, July 1997; 32, 1079–1090.
5. S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMOS Technologies. New York: Springer-verlag, 2006.
6. K.Bernstein et al., “Design and CAD challenges in sub-90nm CMOS technologies,” *in Proc. int. conf. comput. Aided Des.*, 2003; 129-136.
7. “International Technology Roadmap for Semiconductors,” Semiconductor Industry Association, 2005.

8. H.Felder and J.Ganger,"Full Chip Analysis of Leakage Power Under Process variations, Including Spatial Correlations, "in *proc. DAC*, June2005; 523-528.
9. Jun Cheol Park and Vincent J. Mooney" Sleepy Stack Leakage Reduction" *IEEE transactions on very large scale integration (vlsi) systems*, November 2006; 14 (1).
10. Harmander Singh, Kanak Agarwal, Dennis Sylvester, Kevin J. Nowka,"Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating,"*IEEE Transactions on VLSI Systems*, November2007;15(11).
11. Y.Chang.S.K.Gupta, and M.A.Breuer, "Analysis of ground bounce in deep sub-micron circuits", in proc.15th IEEE VLSI Test symp.,1997; 110-116.
12. N.West. K.Eshragian, Principles of CMOS VLSI Design: A systems Perspective, Addison-wesley,1993.
13. Suhwan Kim, Chang Jun Choi, Deog-Kyoon Jeong,Stephen V. Kosonocky, Sung Bae Park," Reducing Ground-Bounce Noise and Stabilizing the Data-Retention Voltage of Power-Gating Structures,"*IEEE transactions on Electron Devices*, January 2008; 55(1).
14. S.Mutoh et al., "1-v power supply high-speed digital circuit technology with multithreshold-voltage CMOS."*JSSC*, Aug.1995; SC-30: 847-854.
15. Charbel J. Akl, Rafic A. Ayoubi, Magdy A. Bayoumi, "An effective staggered-phase damping technique for suppressing power-gating resonance noise during mode transition," *10th International Symposium on Quality of Electronic Design*, 2009;116-119.
16. K. Kawasaki et al., "A sub-us wake-up time technique with bypass power line for rush current support," *IEEE J. Solid-State Circuits* , Apr. 2009; 44 (4): 146–147.
17. Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition, " in ICCD07, pp. 388-394, 2007.
18. M. V. D. L. Varaprasad, Rohit Bapna, Manisha Pattanaik, "Performance Analysis of Low leakage 1-bit Nano-CMOS Based Full Adder Cells for Mobile Applications, " *Proceedings of International Conference on VLSI Design & Communication Systems*, January 2010; 233-238.